Test of Altiroc2 and Altiroc3 at USTC

Zhuang Li, Junzhi Cheng, Yongkang Cai,
Jiajun Qin, Lei Zhao
University of Science and Technology of China

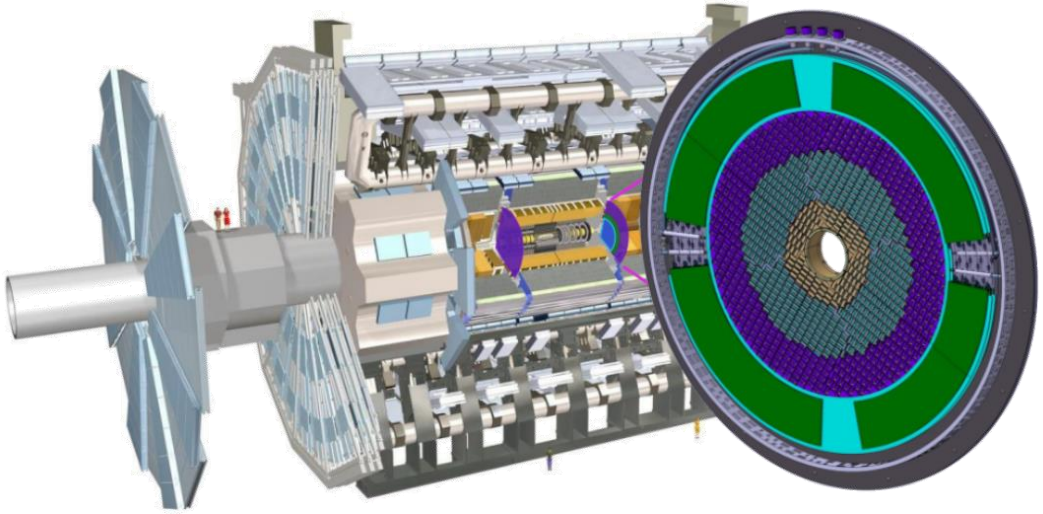
OUTLINE

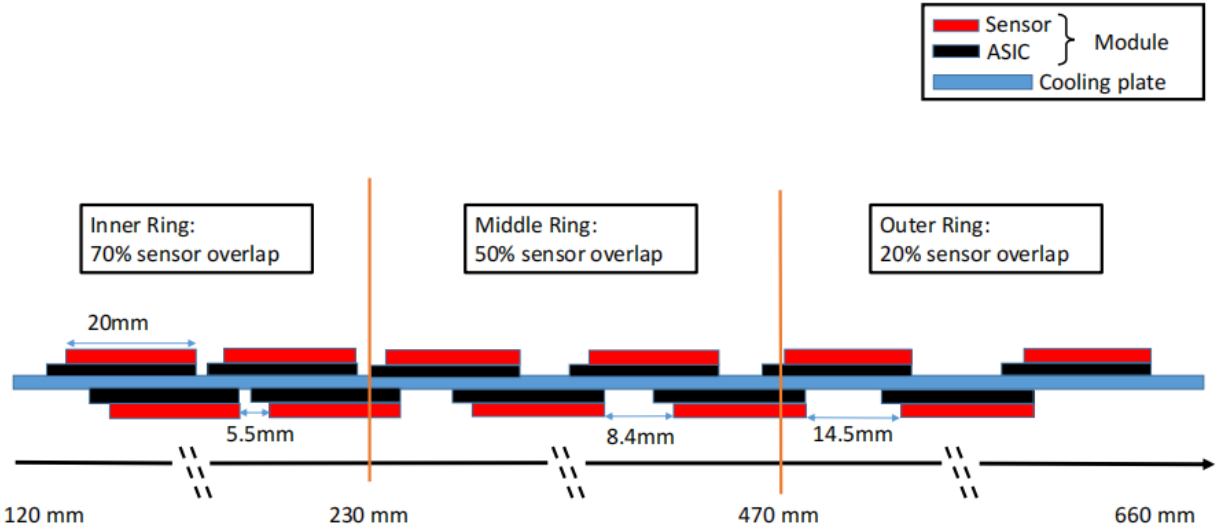
- Background
- Altiroc test system
- Altiroc2 test
- Altiroc3 test
- Summary

LGAD in ATLAS upgrade

- ATLAS plans to use LGAD to achieve high-precision time and position measurement of particles
  - Position: 1.3×1.3 mm^2 spatial position resolution on two disks with a radius of 660 mm
  - Time: 50 ps time resolution for single layer detectors, using double layers near the center for better time precision, 25 ps for electronics
  - Read-out: ASIC bump bonding with LGAD to complete signal processing and time measurement

ALTIROC





LGAD

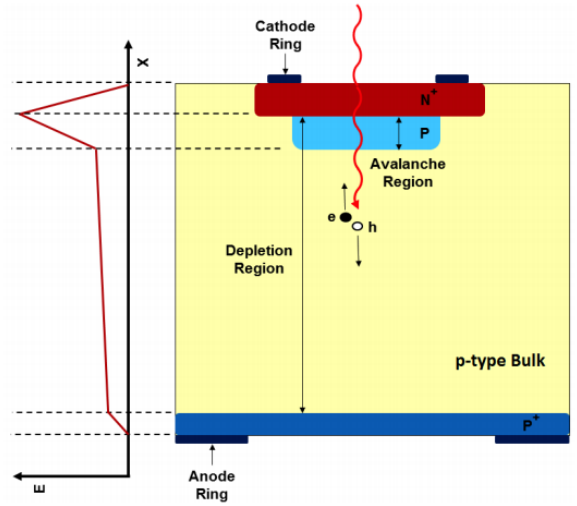
- Basic structure:
  - n-on-p silicon detectors containing an extra highly-doped p-layer
  - The initial current is created by the drift of the electrons and holes
  - New electron/hole pairs are created in the amplification region

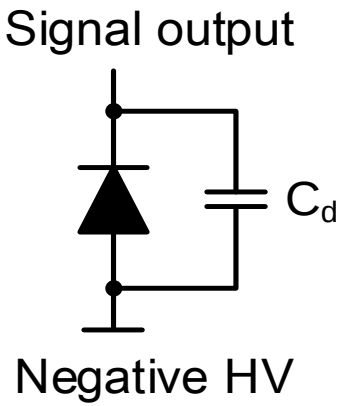
- Electronic characteristics:
  - Rise time： ~ 500 ps
  - Signal duration: ~1 ns
  - Charge: 10fC

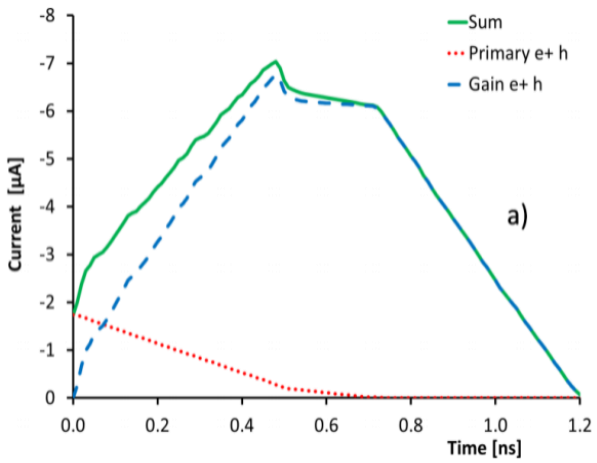
  In Altiroc, the similar signal is generated for test

  - Detector capacitance: ~ 4 pF

Capacitors of the same size are required to simulate the capacitance of the detector in electronic test

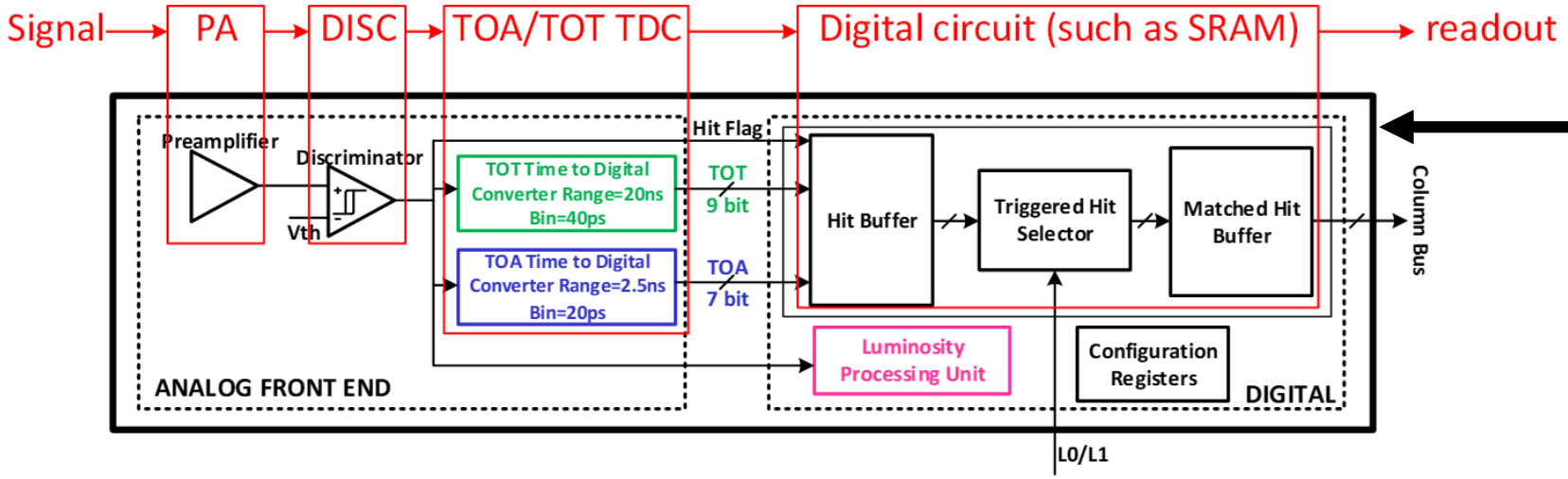


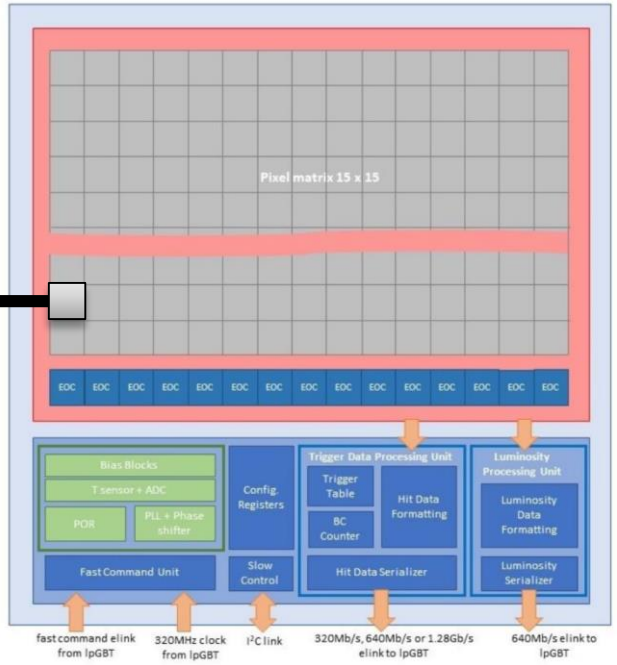




Structure and function of ALTIROC

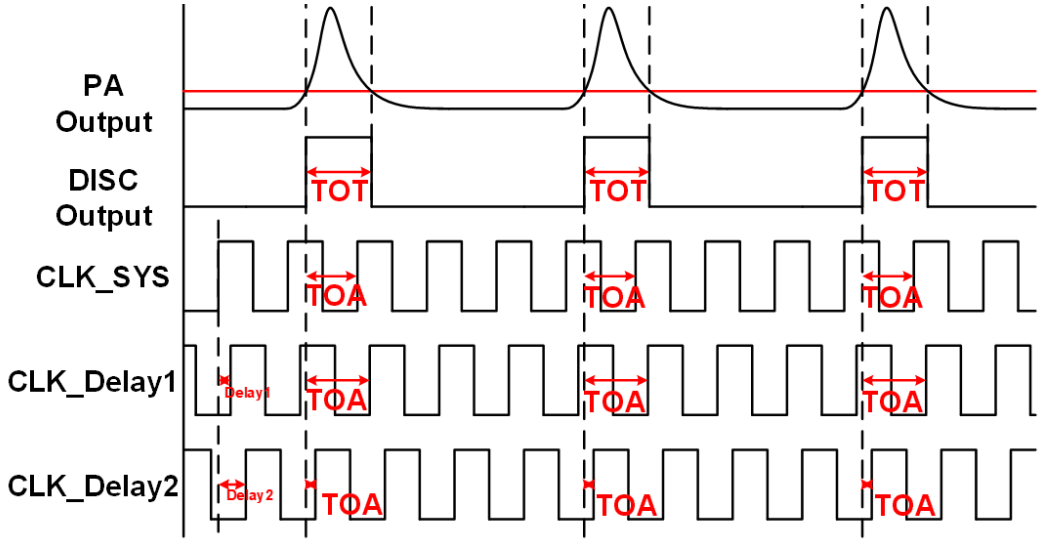
- ALTIROC, ATLAS LGAD Timing Integrated Readout Chip (15×15 channels)
- Pixel architecture: pre-amplifier、discriminator、TDC、digital circuit
- Periphery: bias、clock、slow control、config. registers、trigger data processing、fast command、luminosity processing…
- Function：amplify LGAD output signal、discriminate to obtain pulse-shape signal、measure TOA(time of arrival) and TOT(time over threshold)
- Key performance parameter: time precision

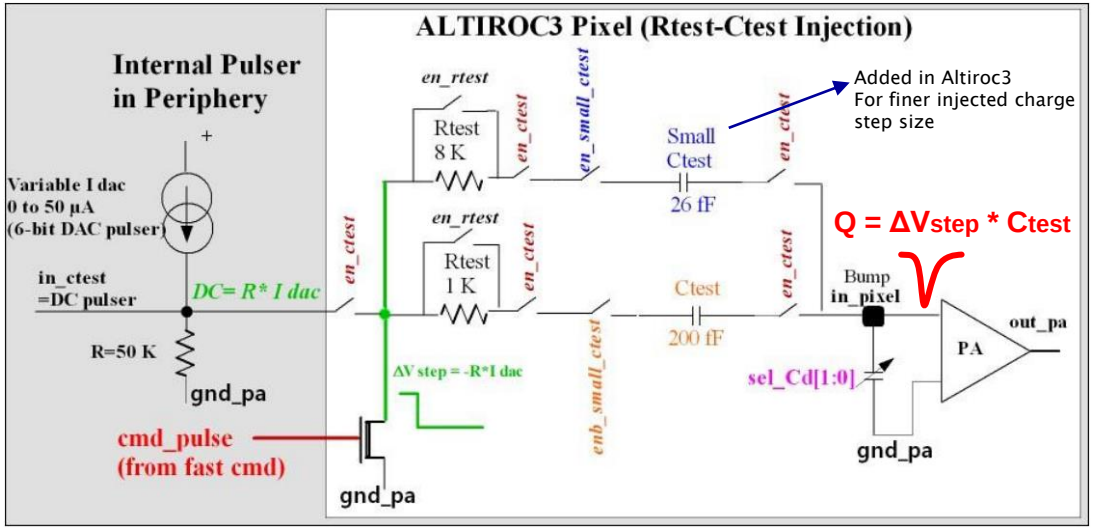


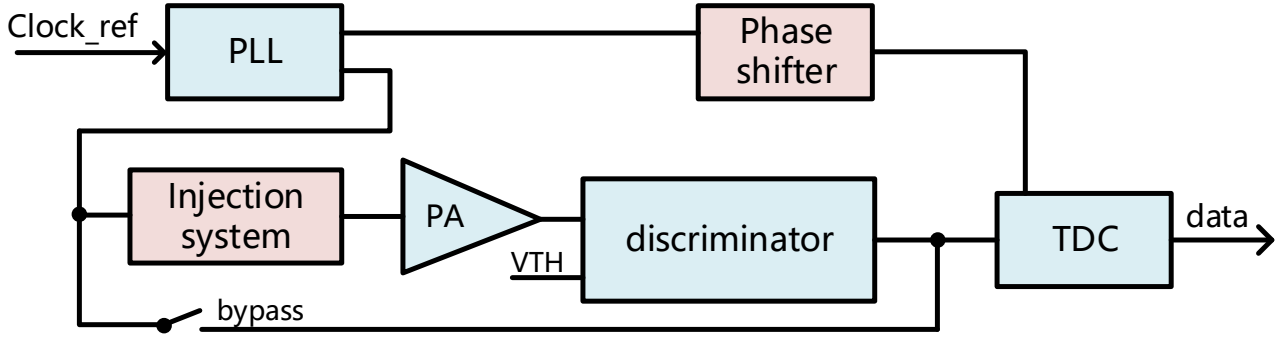


Structure used for testing in ALTIROC

- Injection system
  - Generate test signals similar to LGAD signals
- Phase shifter
  - Change the delay between the test signal and TDC clock





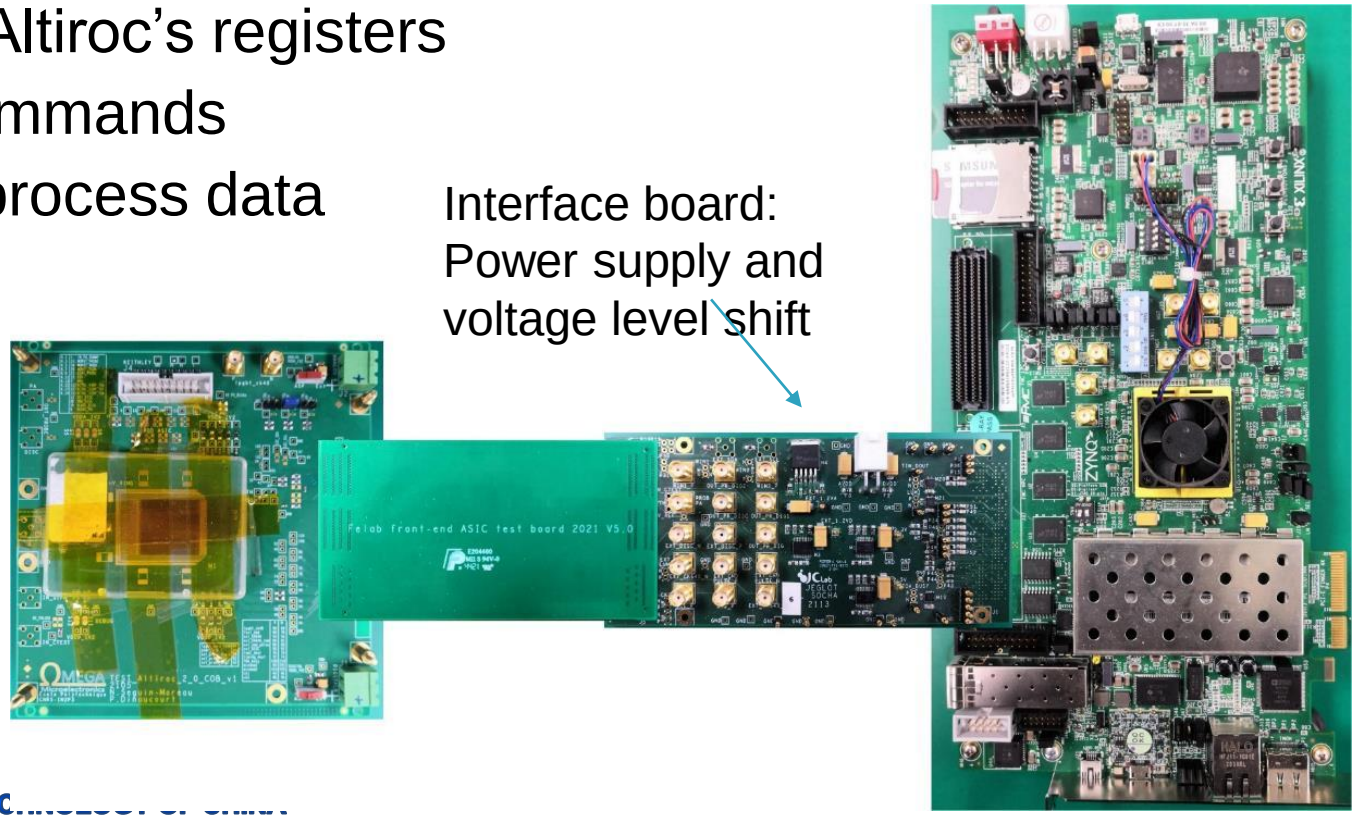


Data acquisition for Altiroc

- FADA, Framework for Altiroc Data Acquisition
  - atlas-hgtd / Electronics / FADA · GitLab (cern.ch)
- FADA runs directly on the embedded CPU in the Zynq board
  - Configurate Altiroc's registers
  - Send test commands
  - Collect and process data

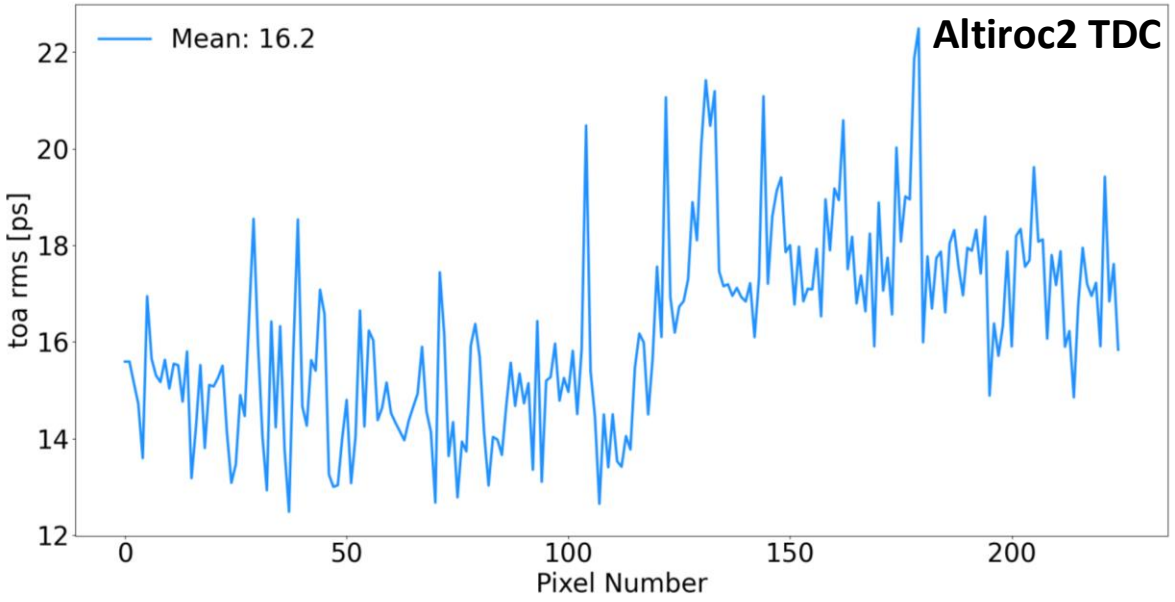
Interface board:
Power supply and
voltage level shift

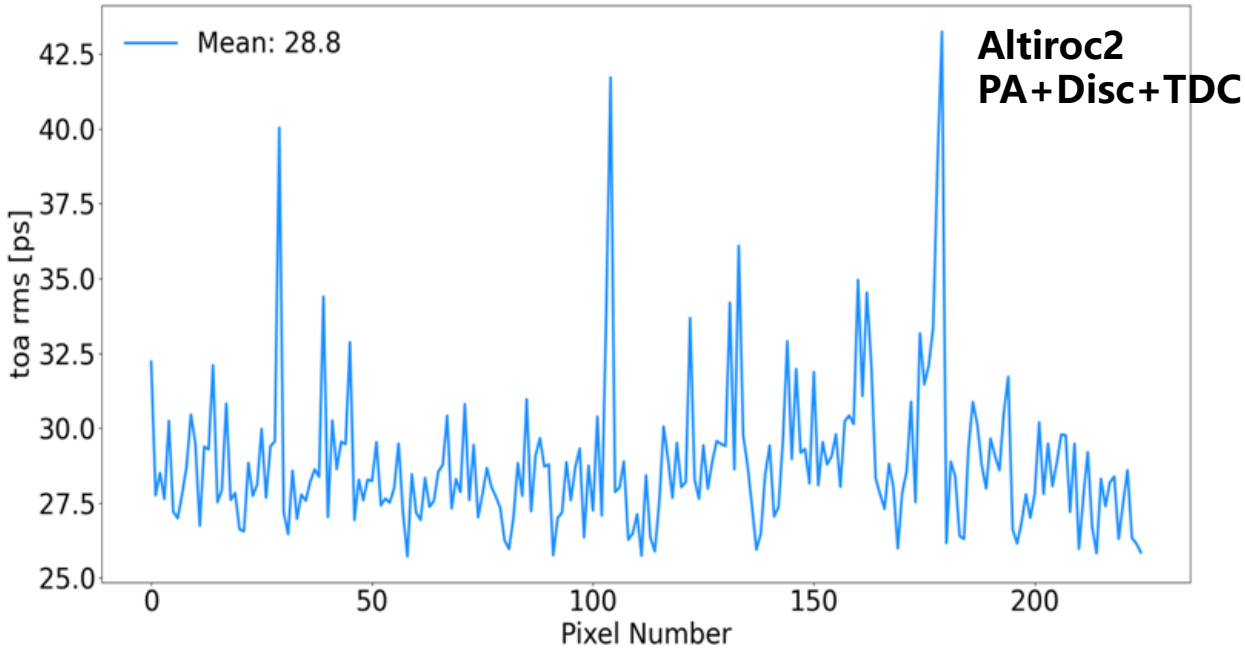
FEE:
Observation points
and bias voltage



Altiroc2 test result

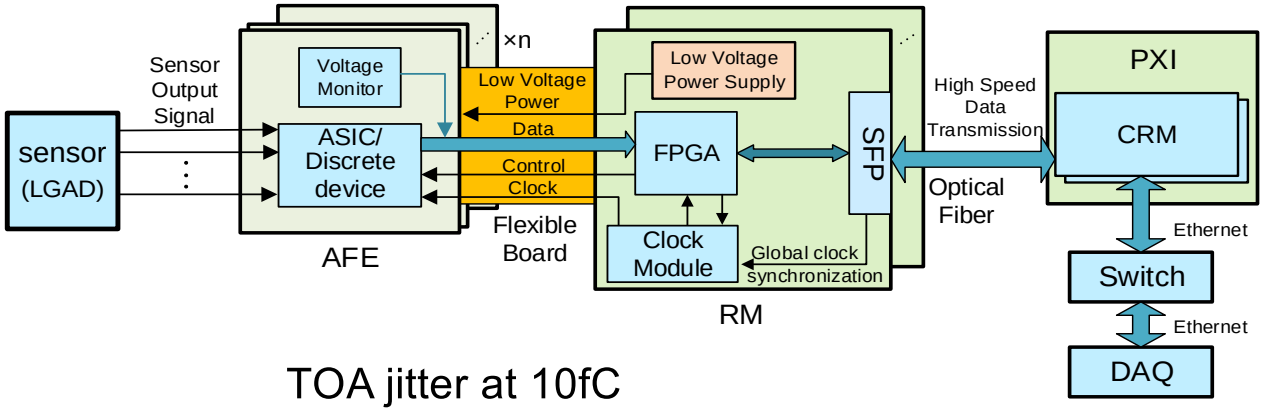
- Based on the FADA system and the FEE provided by OMEGA
  - TDC time precision 16.2 ps
  - Jitter@ 10 fC 28.8 ps

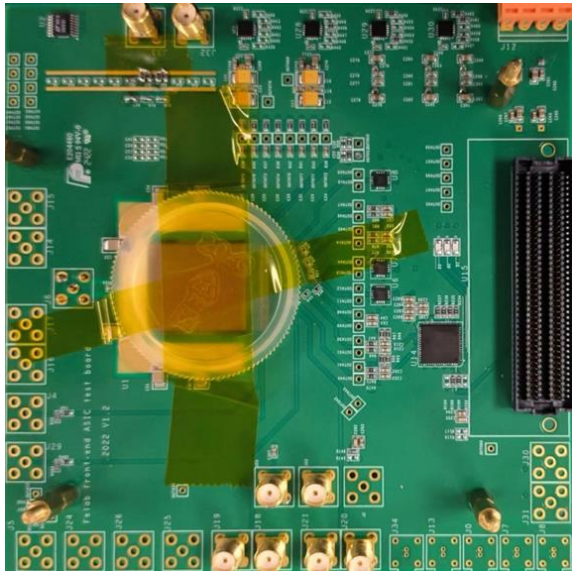


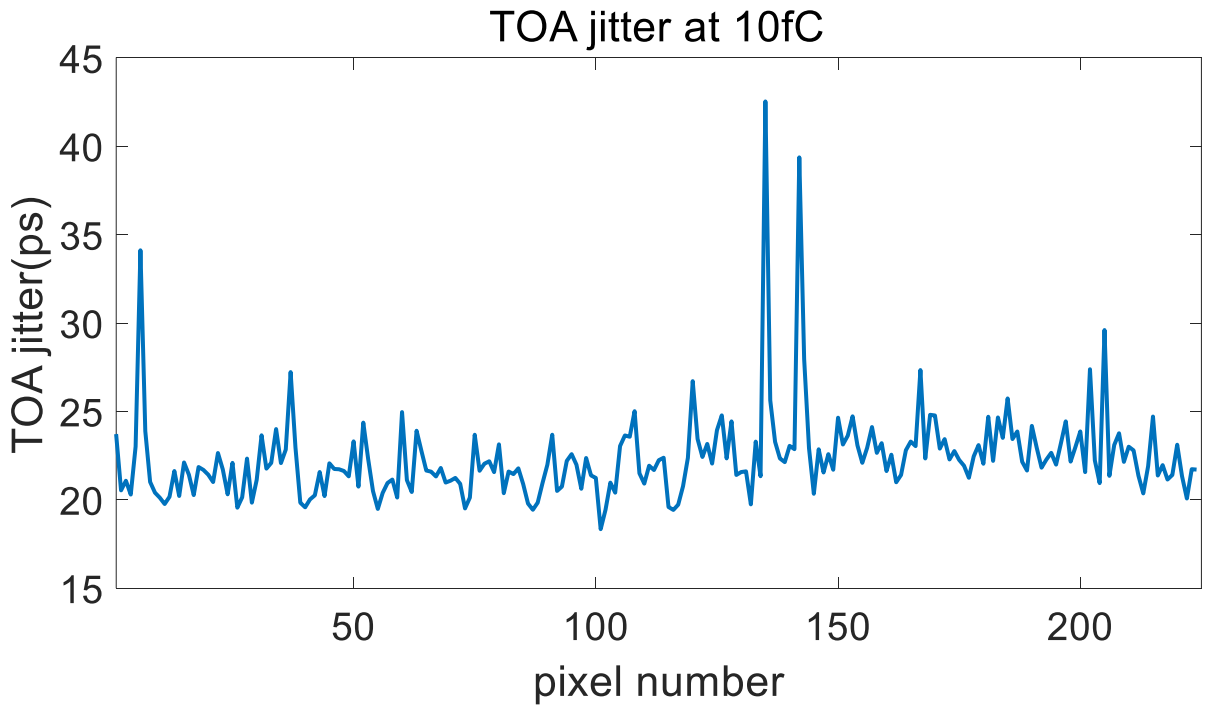


Altiroc2 test result

- Based on self-designed readout system and FEE
  - The TOA jitter of most of channels are better than 25ps @10fC

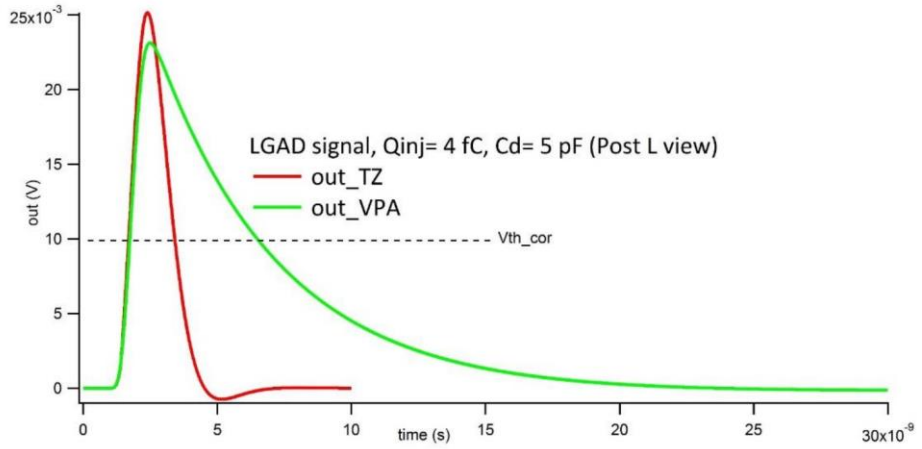


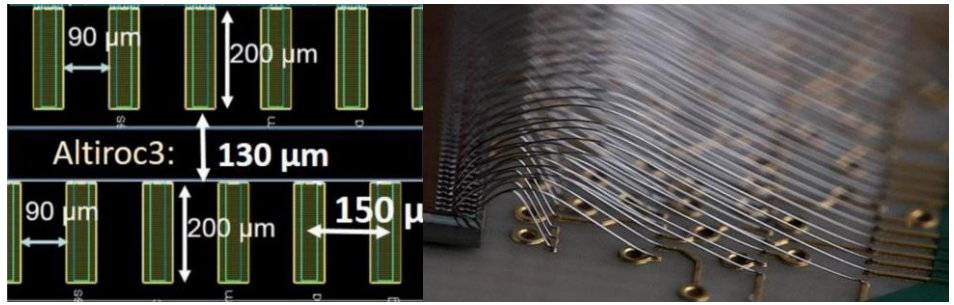




Main difference from Altiroc2 to 3

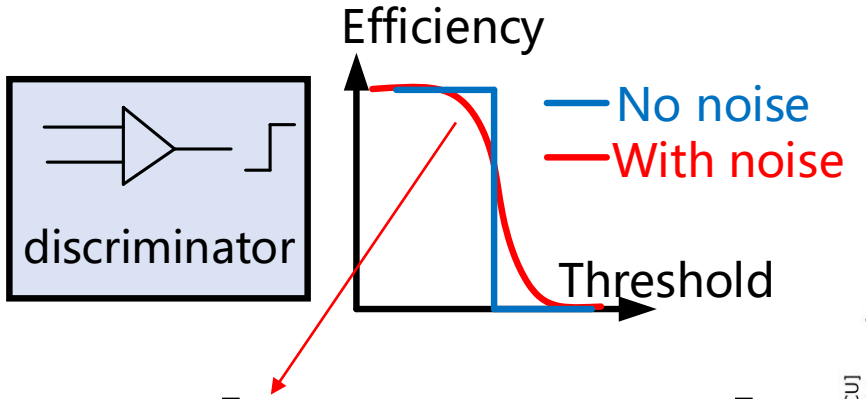
- One type of preamplifier(TZ) is reserved
  - For faster signal edge in trans-impedance architecture
- Add a “small Ctest” in injection system
  - Finer inject charge step size
- Add an internal DAC to set control voltage for delay cells in TDC
  - in case DLLs don’t work properly
- Add more pads for better power supply
  - 263 I/O pads, twice as much as in Altiroc2, most new pads are power pads



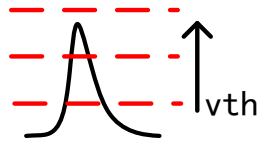


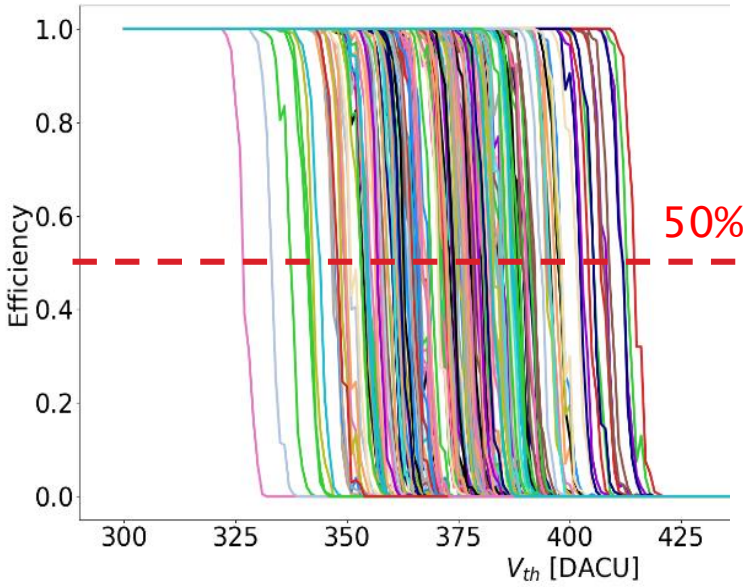
Altiroc3 test: threshold scan

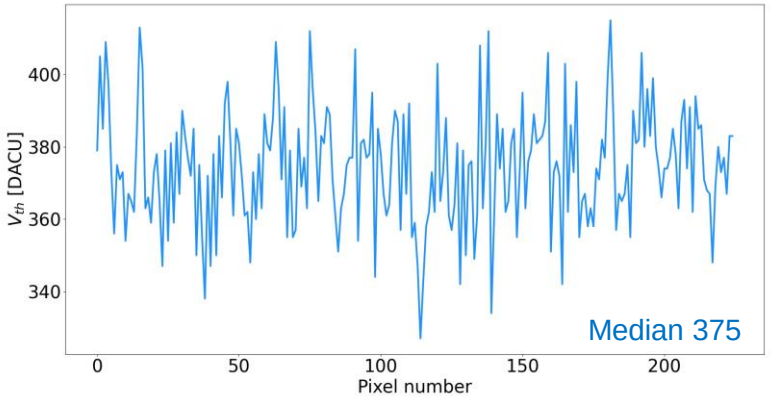
- Inject signal with a fixed amount of charge (5fC, large Ctest)
- The efficiency decreases as the threshold increases
- Define the threshold at 50% efficiency as the signal peak value
- Fitting S-curve to obtain σ（noise in unit of threshold）
- Use the median as the common threshold for all pixels

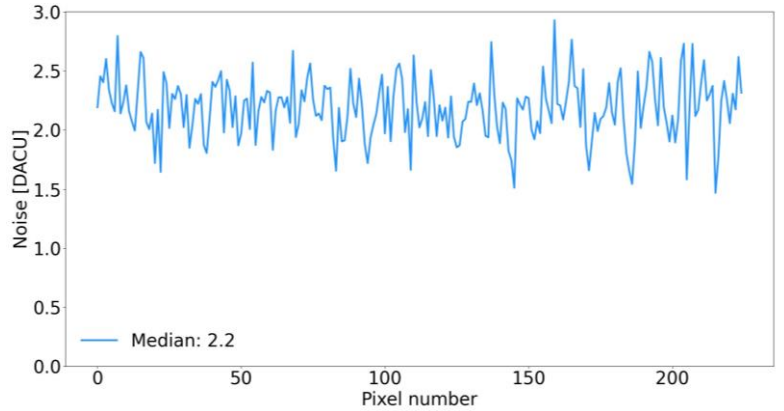


$$P(V_{out}) = \frac{1}{2}\left[1 + Erf\left(\frac{V_{ideal} - V_{threshold}}{\sqrt{2}\sigma_n}\right)\right]$$









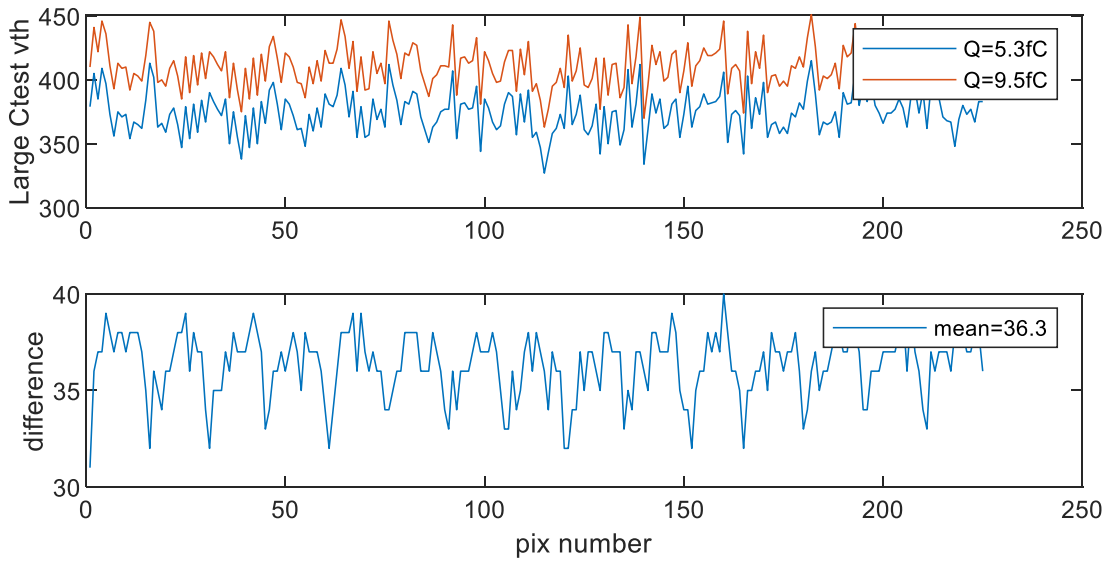
Small Ctest calibration

- Inject signals with different amounts of charge using small / large Ctest respectively
  - Ideally, the ratio of ΔQ is equal to the ratio of ΔVth

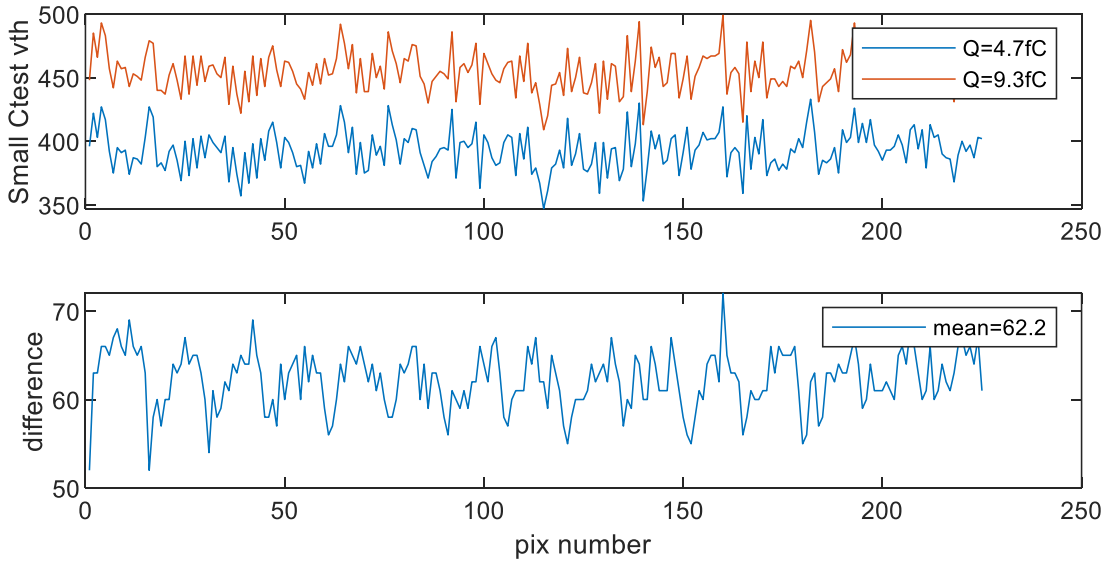
Capacitor mismatch

$$\frac{\Delta Q_{large}}{\Delta Q_{small}} = 0.9 \neq 0.6 = \frac{\Delta vth_{large}}{\Delta vth_{small}}$$

ΔQ = 4.19 fC ΔVth = 36.3



ΔQ = 4.64 fC ΔVth = 62.1

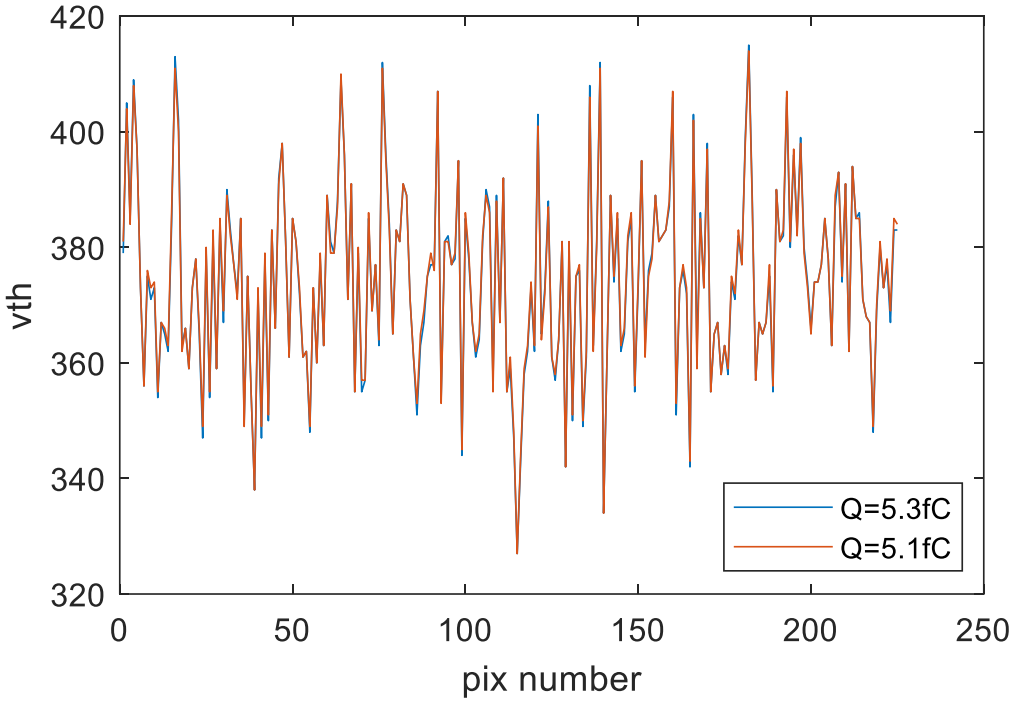


Small Ctest calibration

- Assume that the nominal value is correct for the large Ctest
  - Generally, the mismatch of small capacitor is more obvious
  - Allow direct comparison with ALTIROC2
- $C_{large}/C_{small} = 5.2 \Rightarrow C_{small}=40$ fF

$$\frac{C_{large}}{C_{small}} = \frac{\Delta DAC_{SC} * slope_{HR}}{\Delta DAC_{LC} * slope_{LR}} * \frac{\Delta Vth_{LC}}{\Delta Vth_{SC}}$$

Ctest	Idac	Vth_mid	charge
Large	12	375	5.3 fC
Large	24	411	
Small	87	394	
Small	110	455	
Small	80	375	5.1 fC

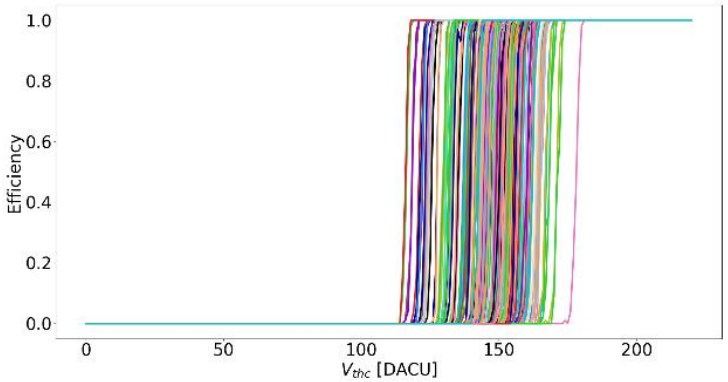


Use the calibrated small capacitor value to inject a 5fC charge, the result is basically coincide with large capacitor

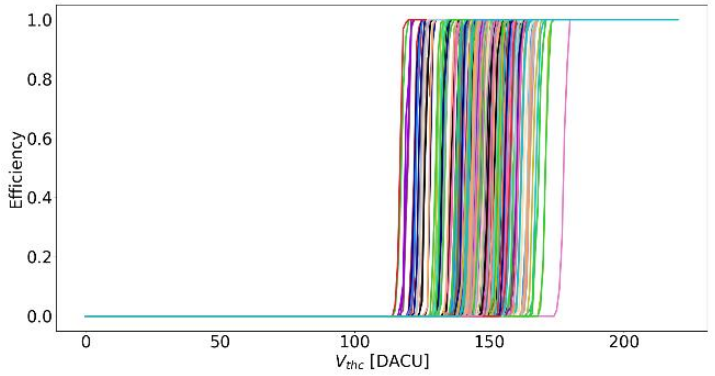
Calculate with calibrated Small Ctest

Pixel threshold correction

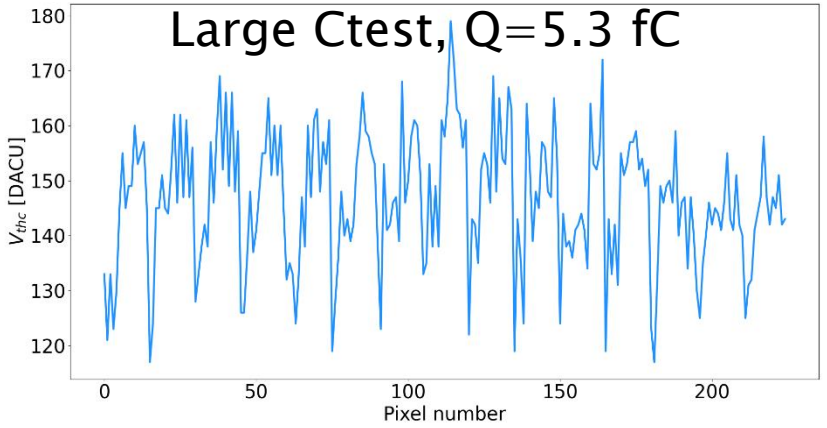
- For each pixel, a local 8-bit DAC correction (vthc) is used to compensate for the non-uniformity
- Set common threshold to the median of each pixel and change vthc to calibrate it
- The calibrated threshold is the peak value of ~5fC signal, which will be used for following test

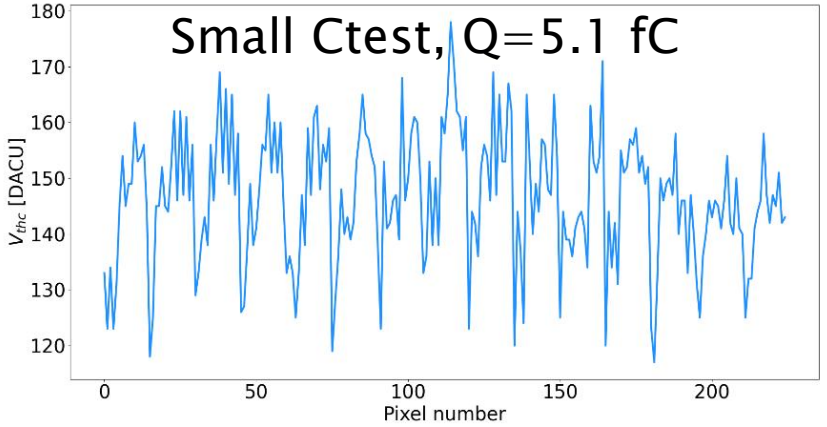


Large Ctest, Q=5.3 fC



Small Ctest, Q=5.1 fC

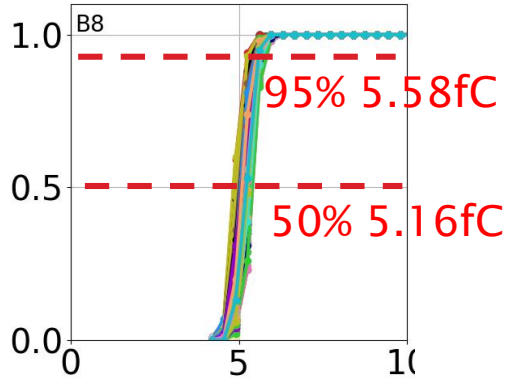




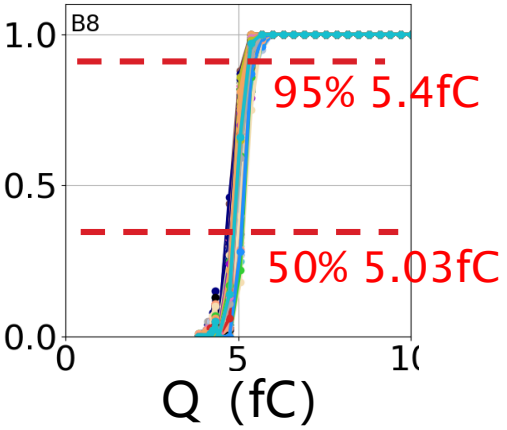
Charge scan

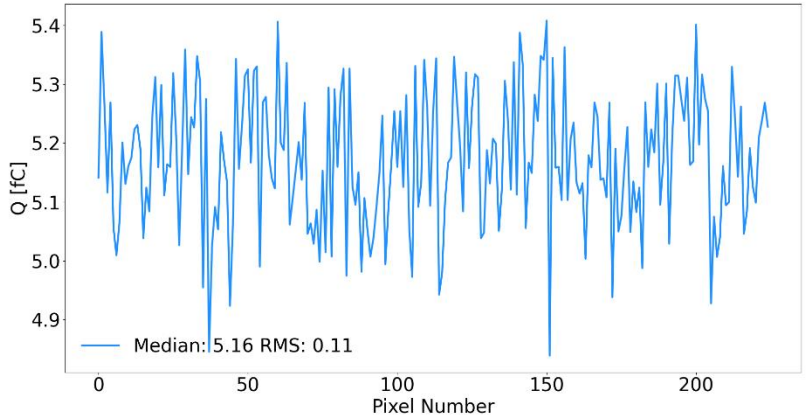
- S-curves gather together, indicating that the previous calibration was right
- Minimum detected charge(95% efficiency): 5.58 fC / 5.4 fC
- ENC 0.26 fC / 0.21 fC

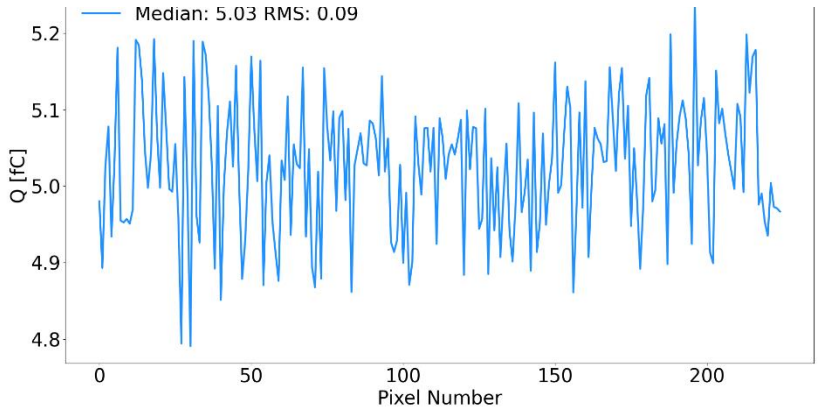
Small Ctest

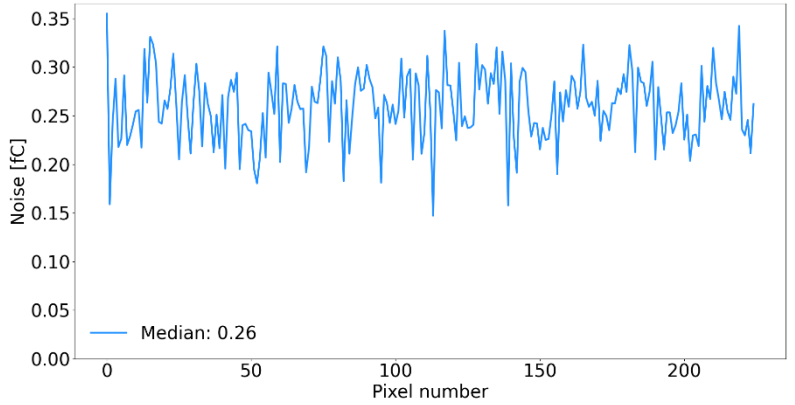


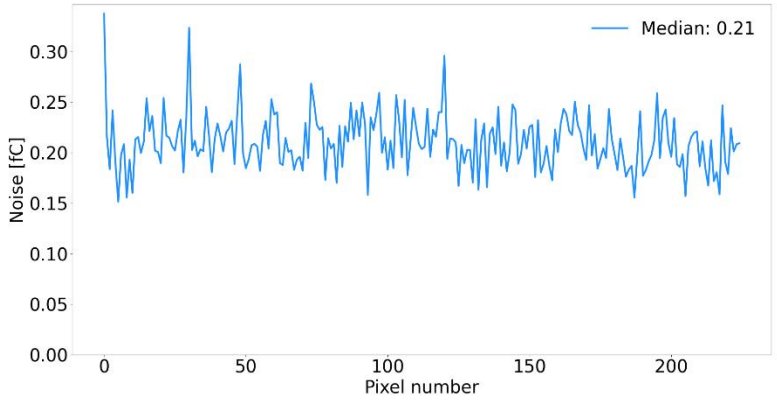
Large Ctest





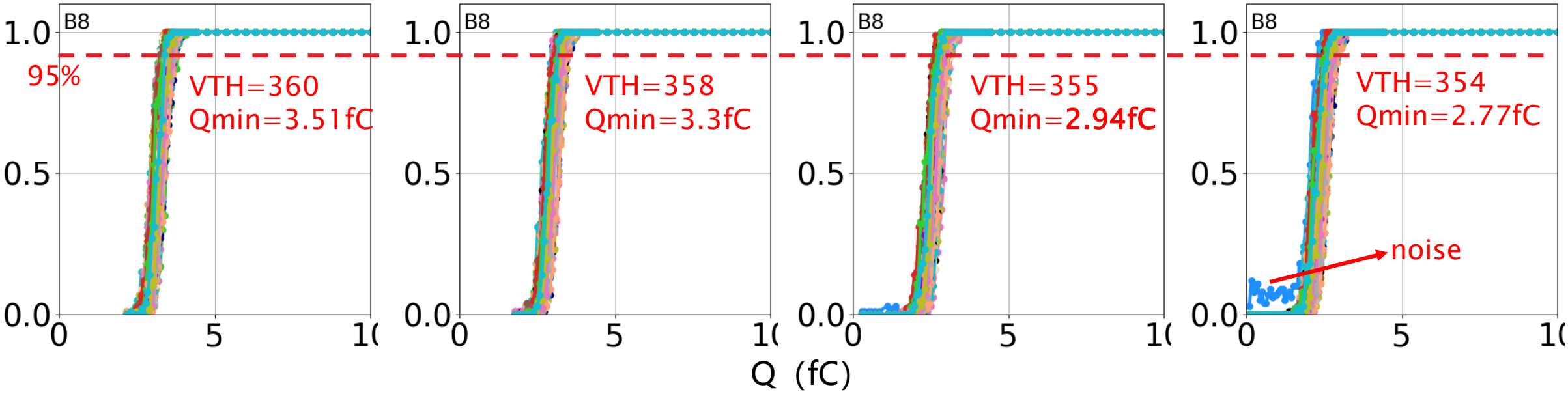






Minimum detected charge

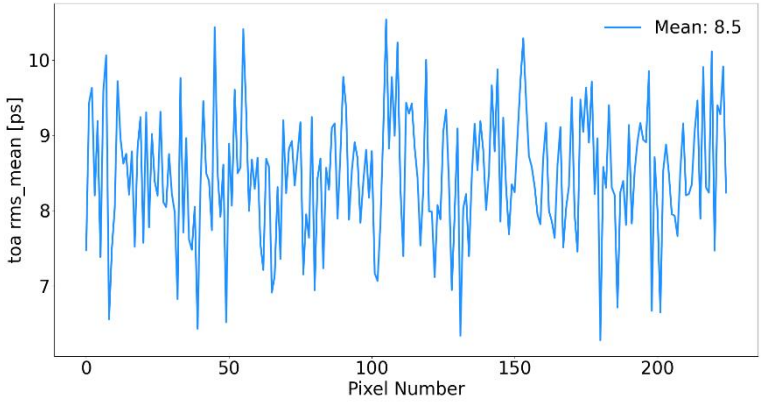
- Calibrate vth and vthc with a smaller charge (3.1fC)
- Gradually reduce the threshold until the noise on the baseline is identified
- Qmin = 2.94 fC ENC = 0.22 fC

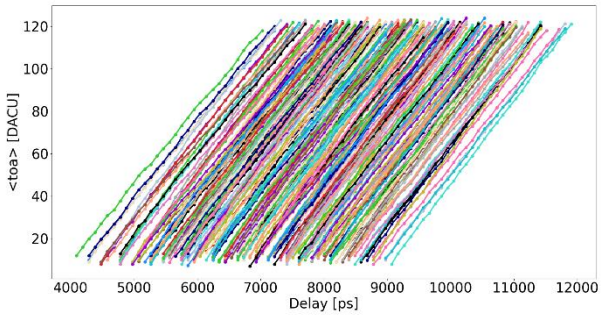


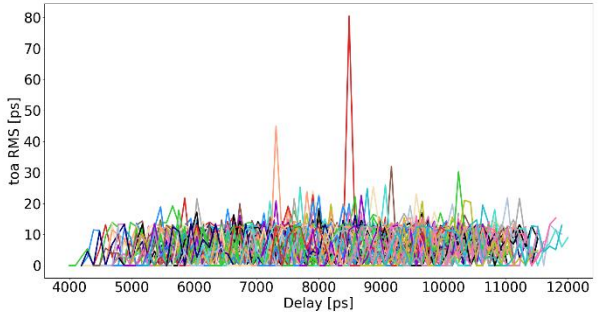
Use small Ctest for smaller ΔQ steps during this process

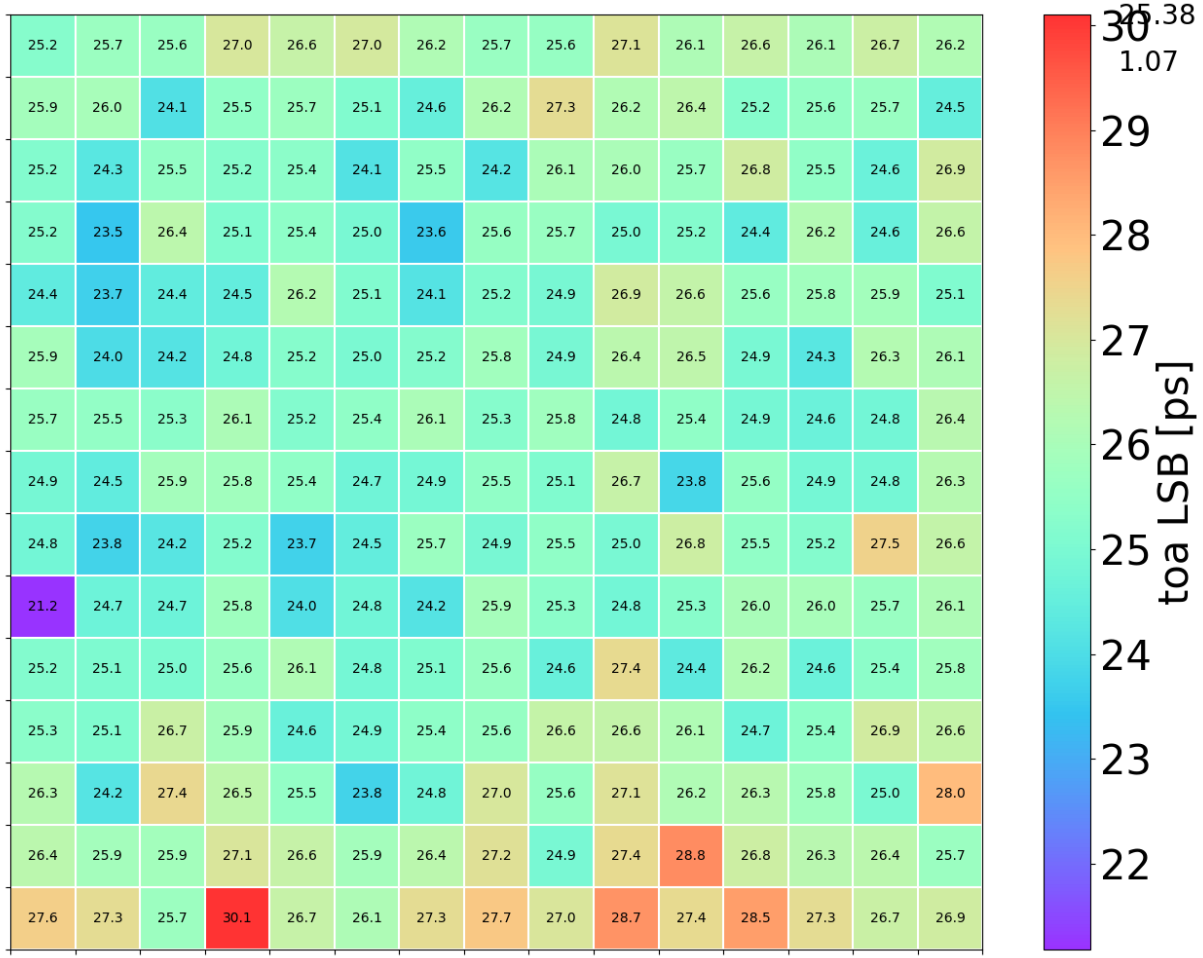
TDC delay scan

- Use phase shifter to change the delay of the TDC clock, calibrate bin size and test the time precision of TDC
- Bin size ~25 ps
- TDC jitter mean 8.5 ps



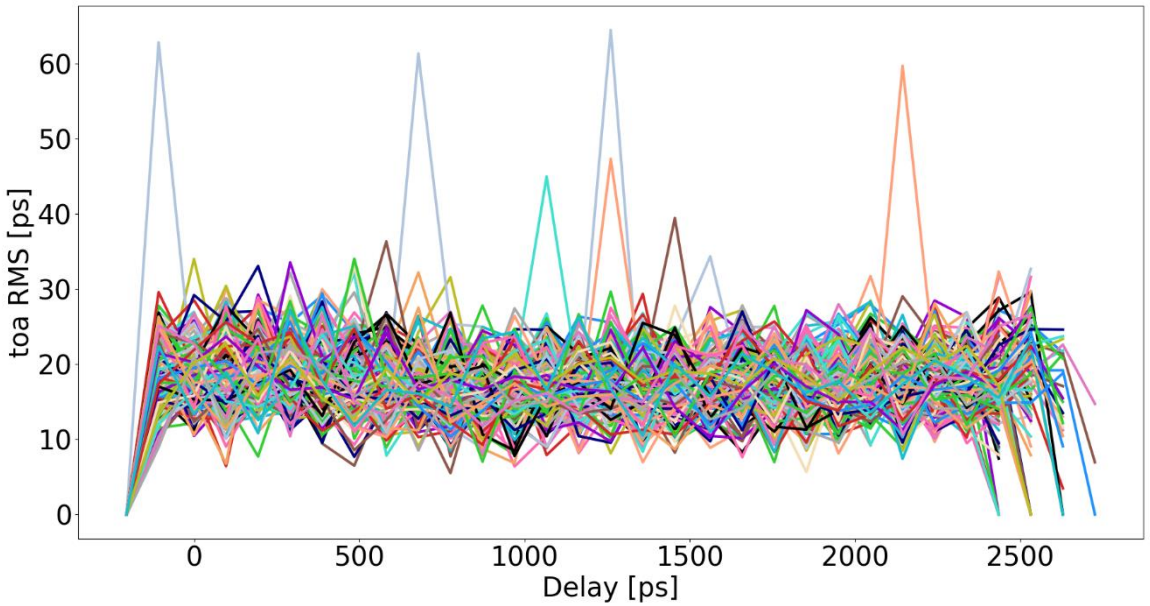


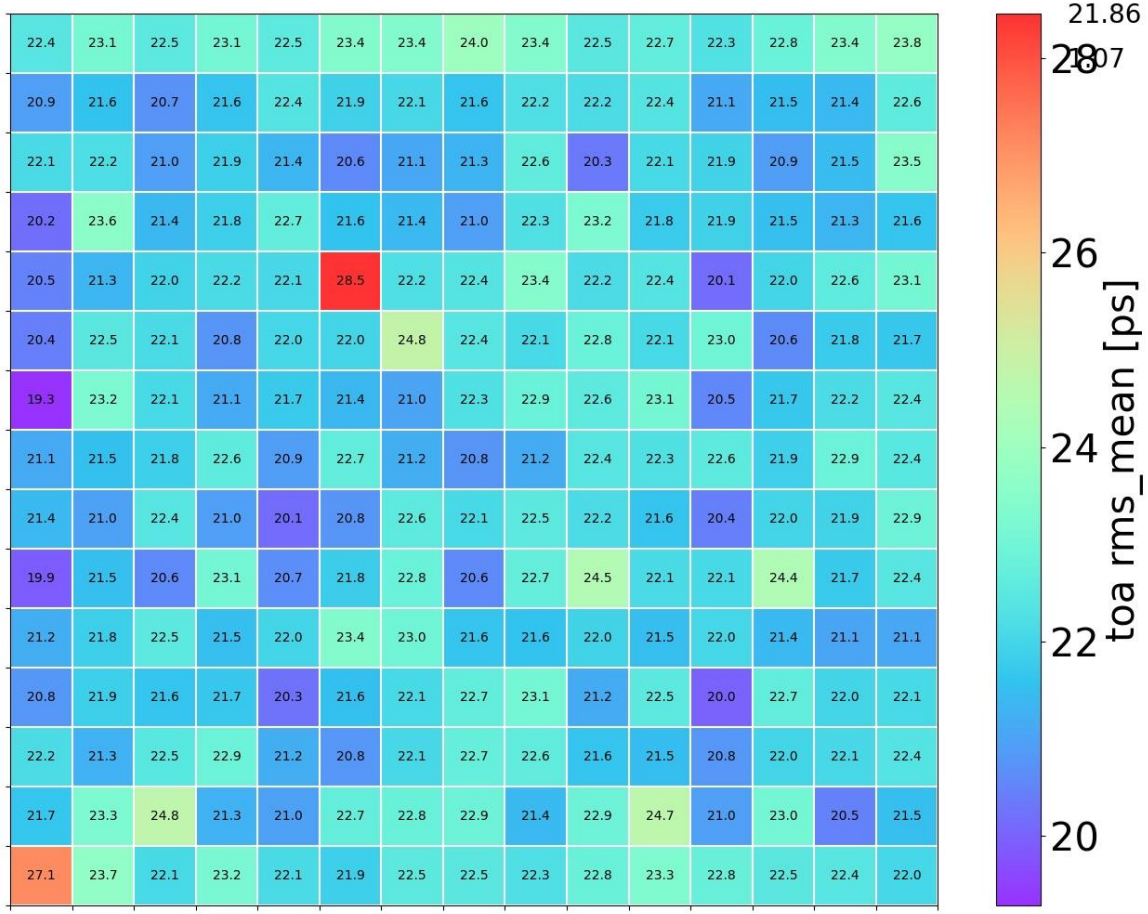




TOA jitter @10fC

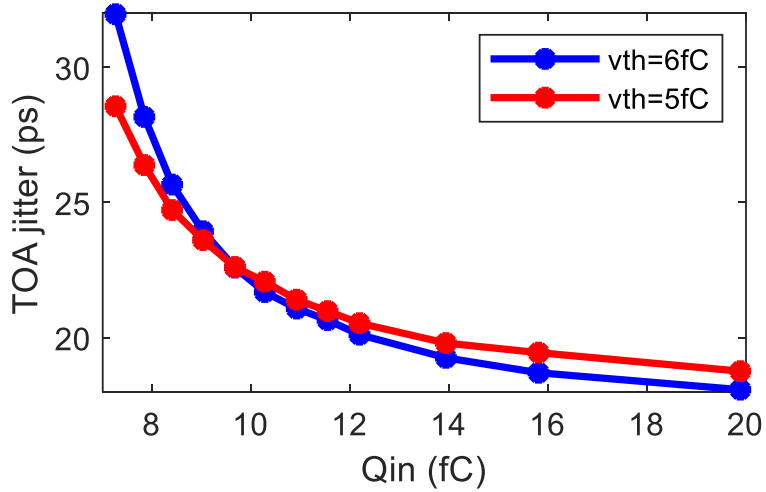
- Inject a charge of 10fC and use 5fC as the threshold to test the TOA jitter of electronics.
- TOA jitter: 22 ps
  - (mean of all pixels, all delays@10fC 3pF)

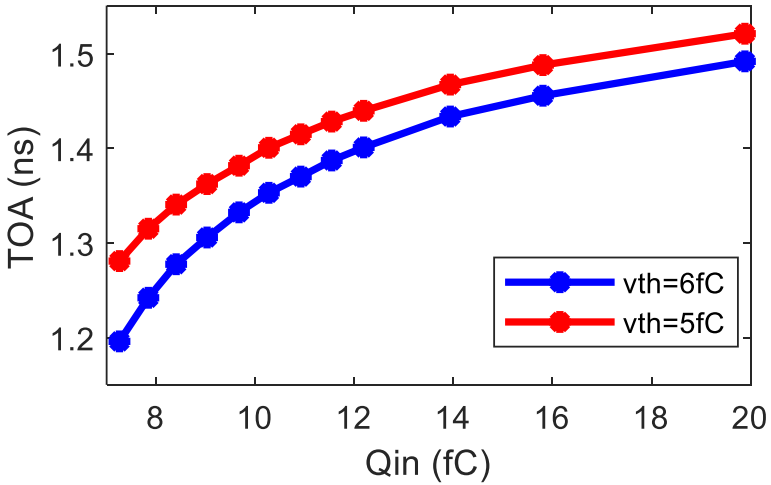


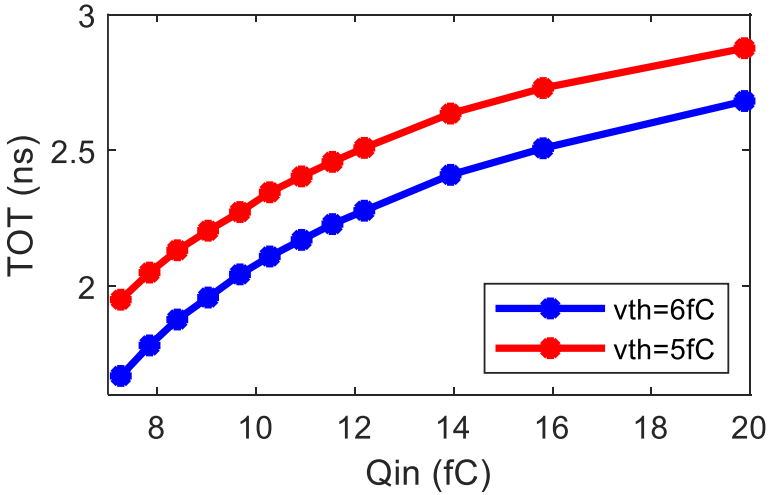


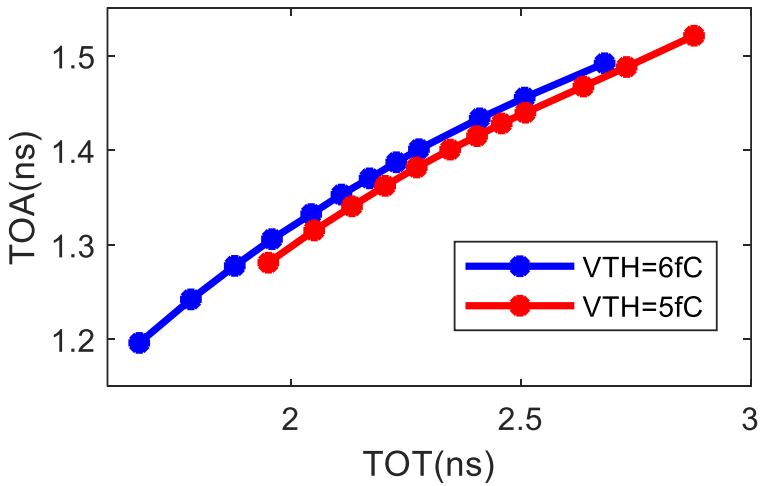
TOA, TOT changing with charge

- The jitter decreases as the amount of charge increases
- TOA(at a fixed delay) increases as the amount of charge increases (time-walk effect)
- The curve between TOT and TOA is monotonous and smooth, so TOT can be used for time-walk correction









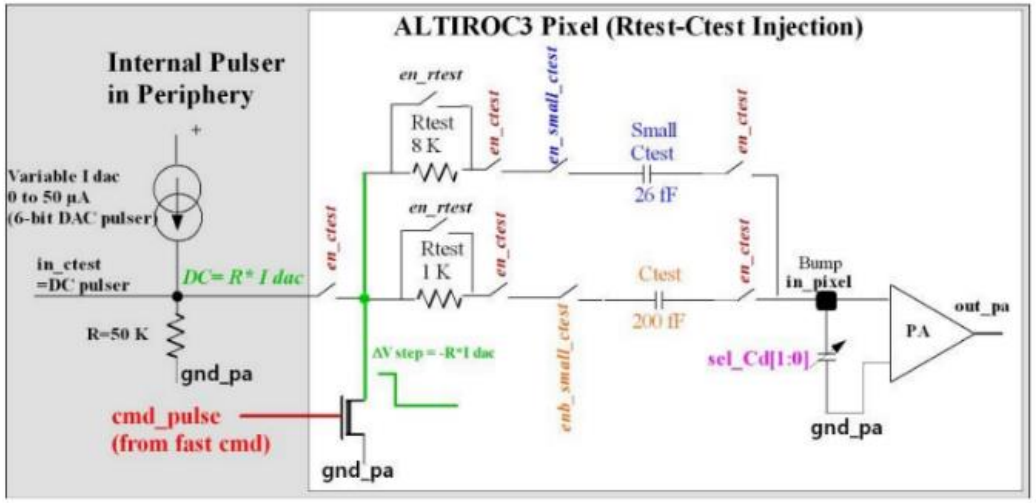
Summary

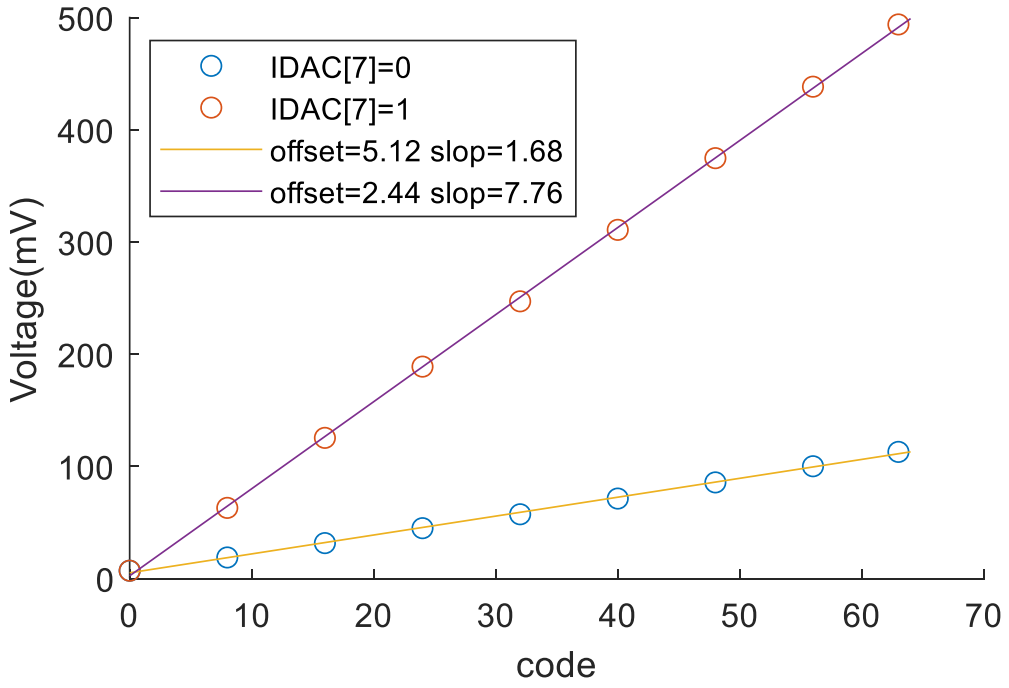
- Built the testing system for Altiroc
- Completed the main performance indicators testing of Altiroc2 and Altiroc3
- Test results of Altiroc3
  - ◇Minimum discernable charge: 2.94 fC
  - ◇Equivalent noise charge: 0.22 fC
    - Altiroc2 0.23 fC
  - ◇TDC time precision：8.5 ps
    - Altiroc2 16.2 ps
  - ◇TOA jitter at 10 fC and 3 pF: 22 ps
    - Altiroc2 28.8 ps

BACKUP

Altiroc3 test: Injection system Calibration

- The amount of injected charge is equal to delta step-voltage multiplied by test capacitance $Q = \Delta V_{step} * C_{test}$
- $\Delta V_{step} = R * I_{DAC}$
- Calibrate ΔV_{step}:

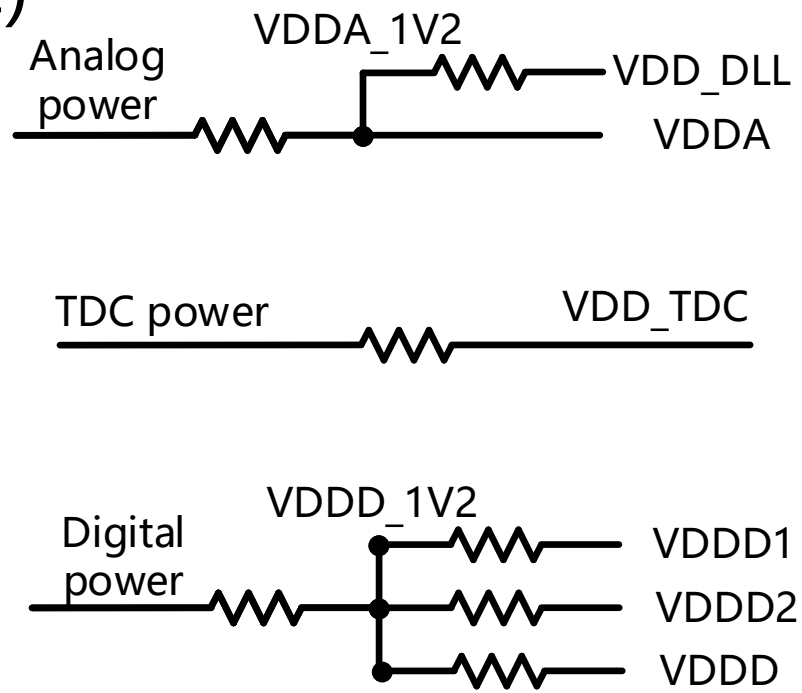




Power Consumption

- Calculate the power consumption by measuring the voltage drop of the 0.1 ohm resistors on the PCB
- Total **640 mW / 840 mW** (static / 160kHz)

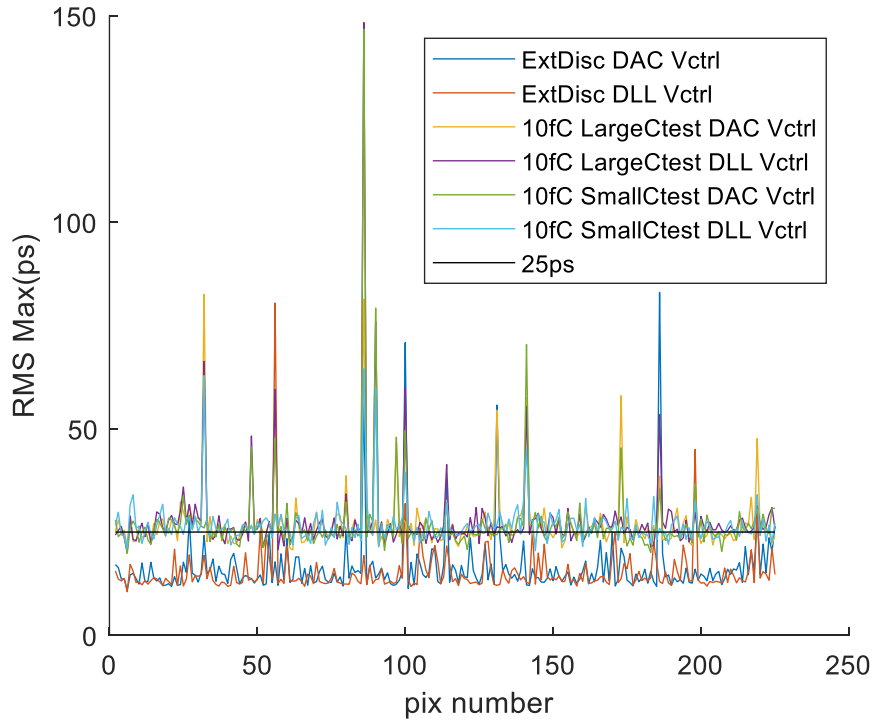
	Static(mA)	160 kHz(mA)
Total	530	700
Analog	90	230
DLL	20	20
Digital	400	420
VDDD1	20	30
VDDD2	310	320
VDDD	20	30
TDC	40	50

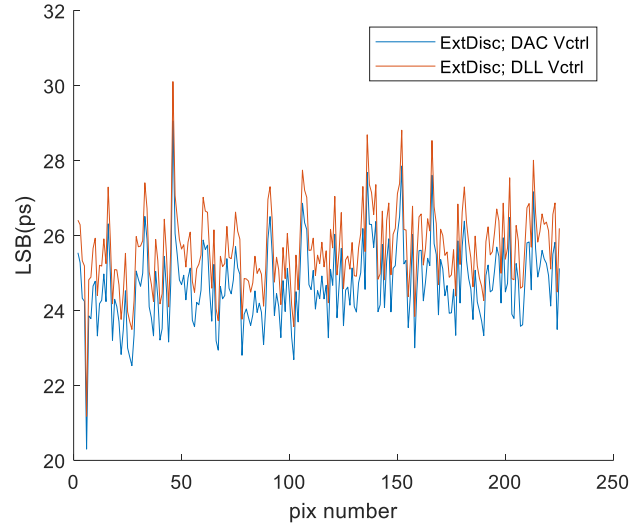


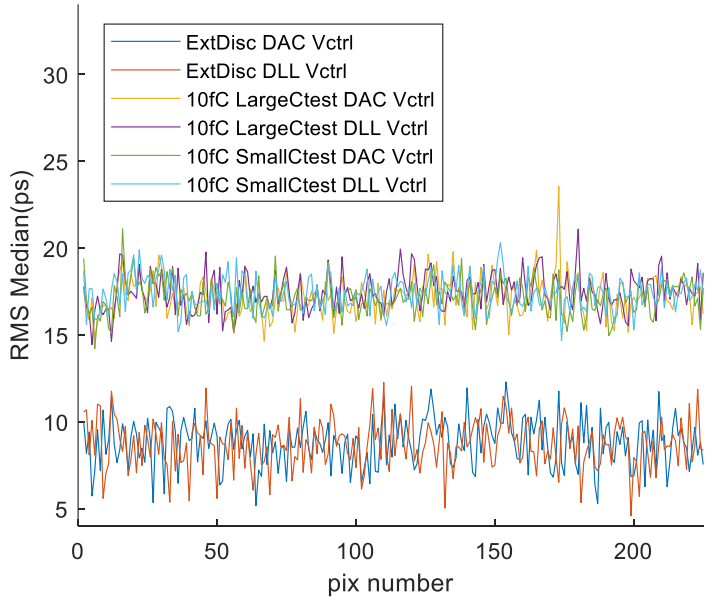
All resistances are 0.1 ohm

Delay scan in different situations

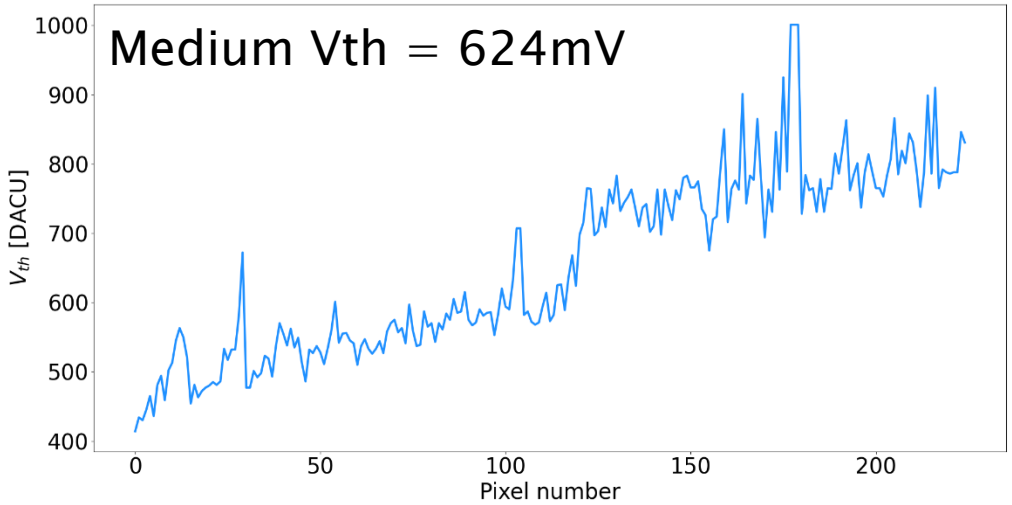
- Not much difference using small or large Ctest、 DAC or DLL Vctrl



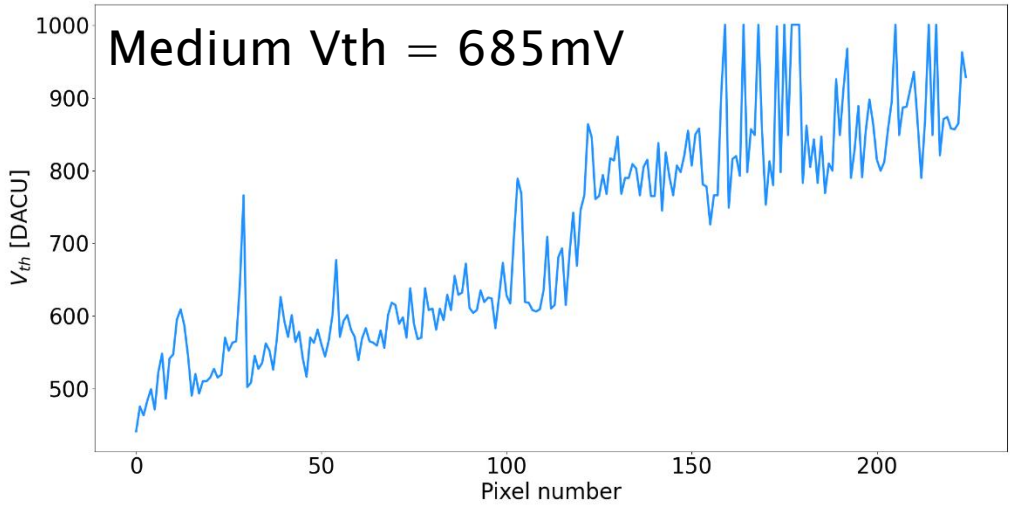




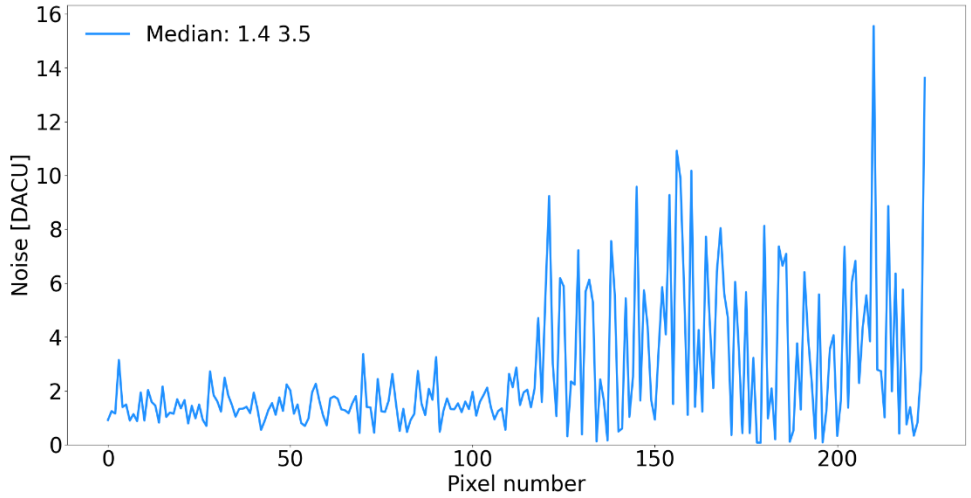
Vth Scan



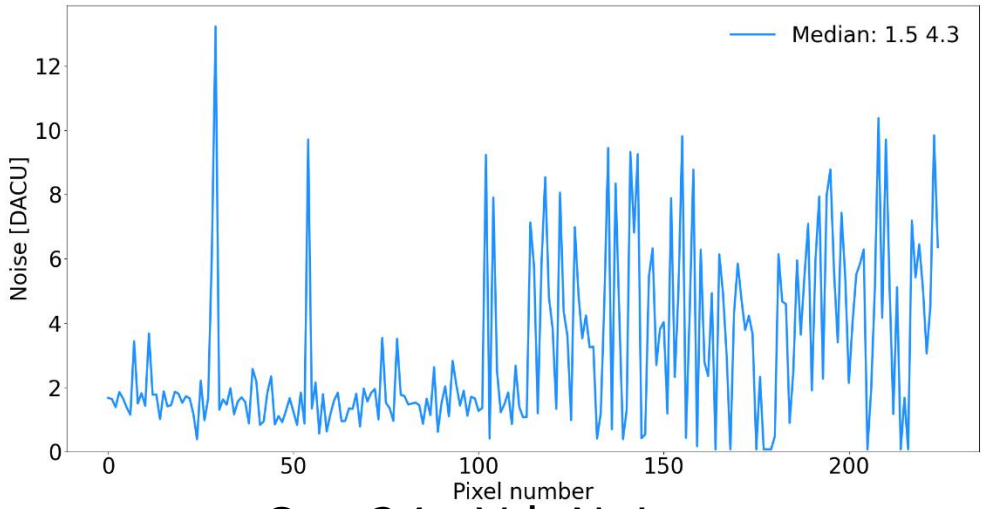
Q = 12 , Vth@50% efficiency



Q = 24 , Vth@50% efficiency

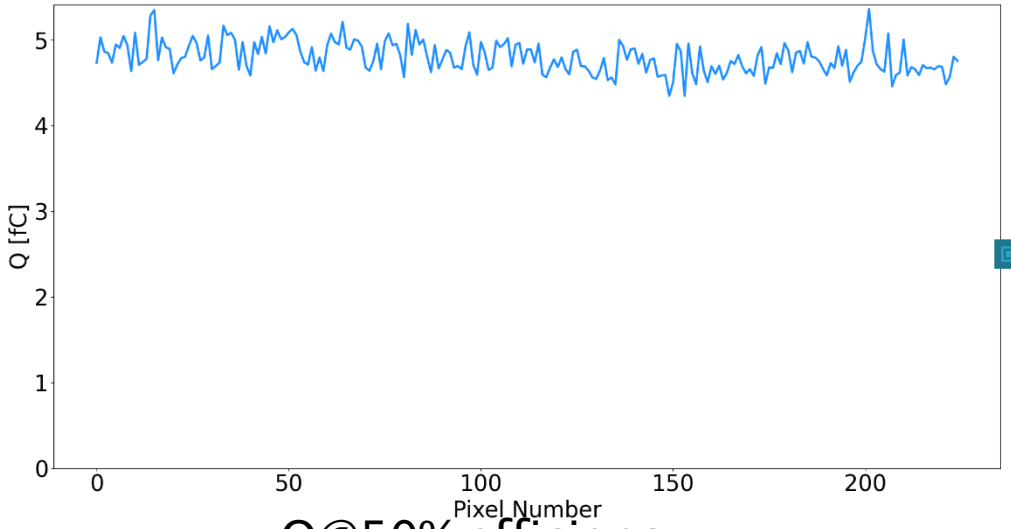


Q = 12 , Vth Noise

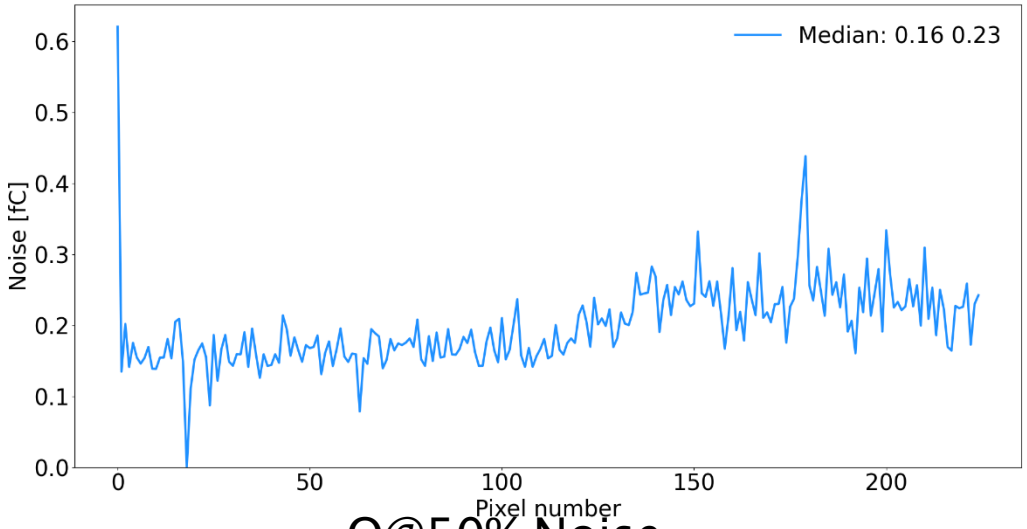


Q = 24 , Vth Noise

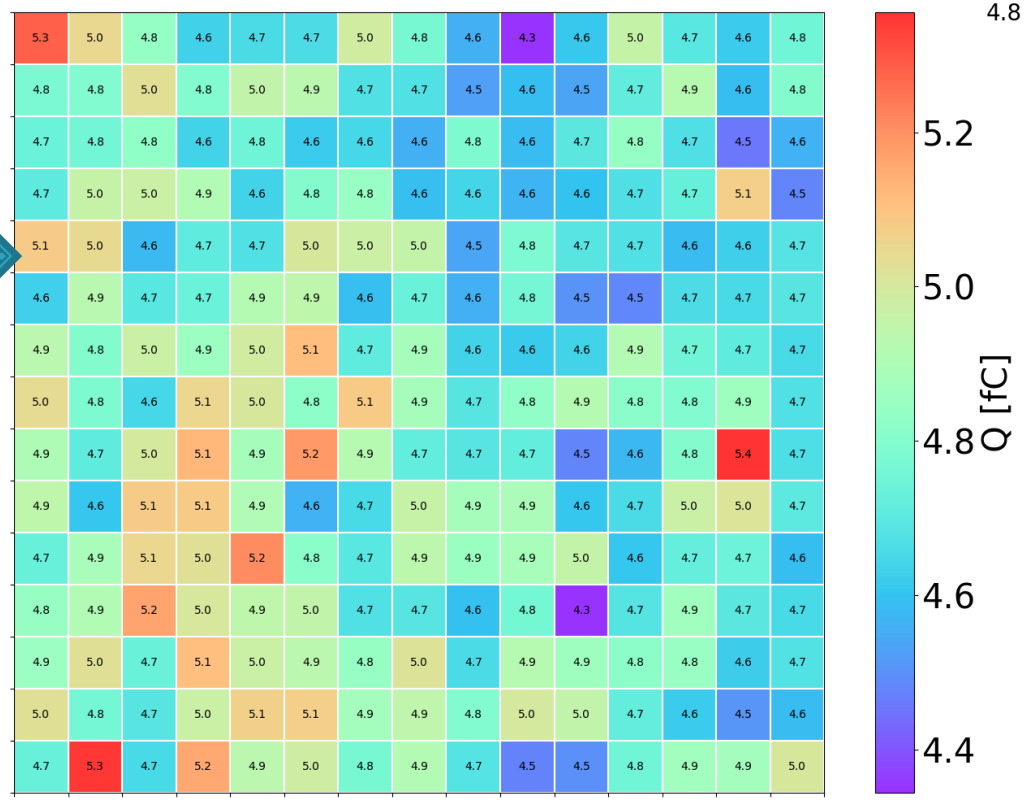
Charge Scan



Q@50% efficiency



Q@50% Noise



Q@50% efficiency