HGTD module assembly and module test at USTC

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On behalf of USTC HGTD group

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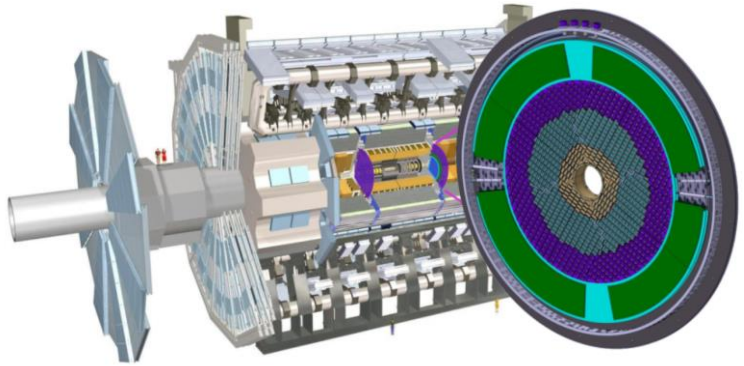
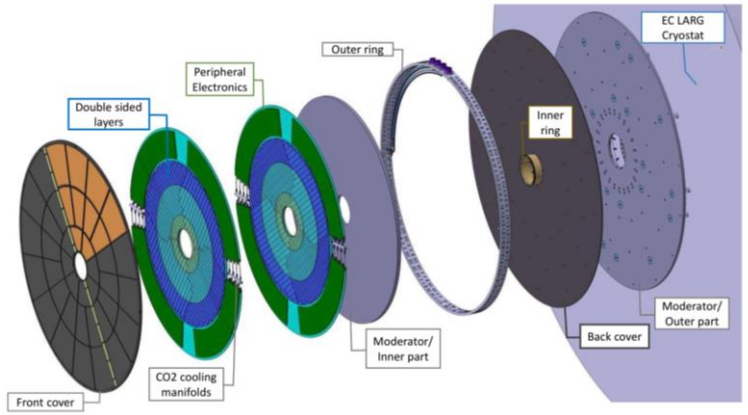
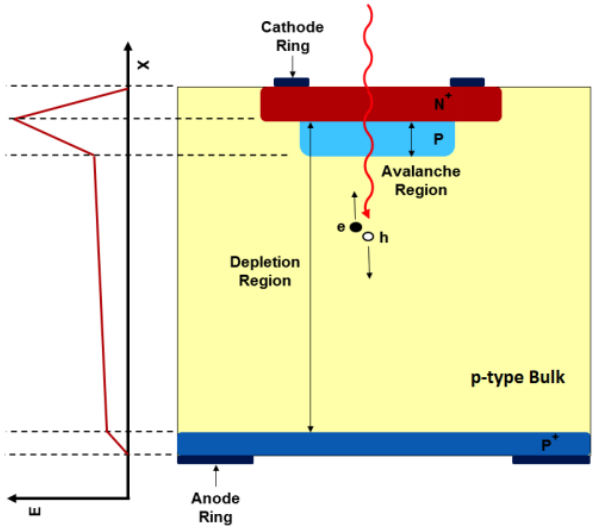
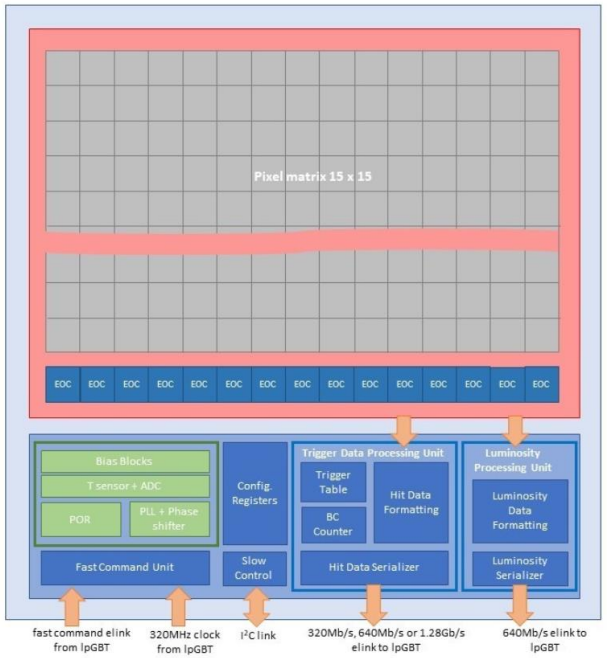
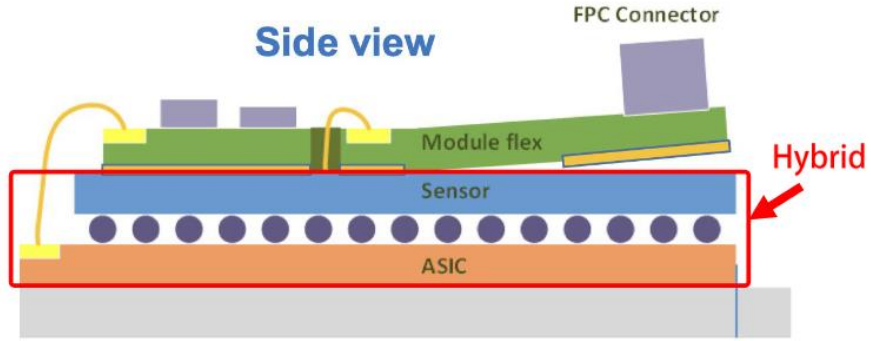
Motivation











- The High Granularity Timing Detector (HGTD) will provide time information in the forward region.
- By using high-precision timing information, the increase of pileup interaction from LHC to HL-LHC can be mitigated powerfully.
- The sensor will be the Low Gain Avalanche Detector (LGAD).
- The front end electronic ASIC is named ALTIROC.
- ALTIROC and LGAD will be bump bonded into a hybrid.
- Two hybrids, along with a module flex, will be assembled into a full module.

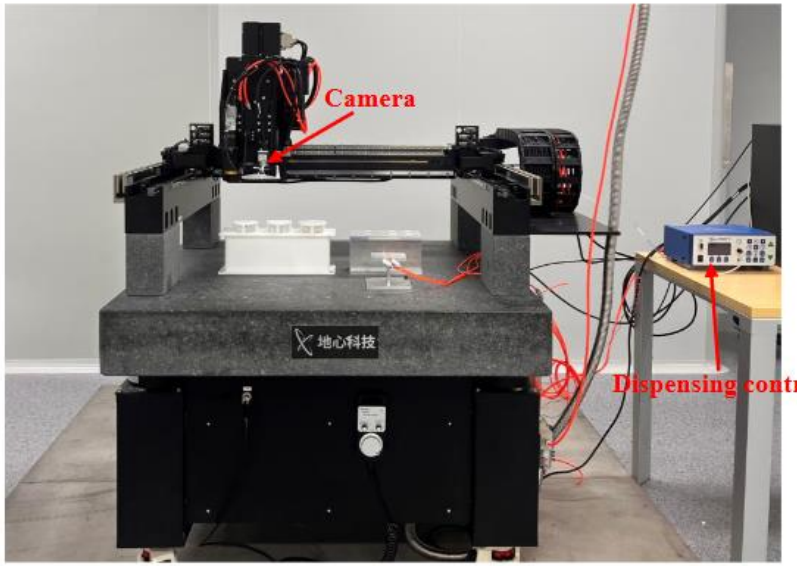
Module Status

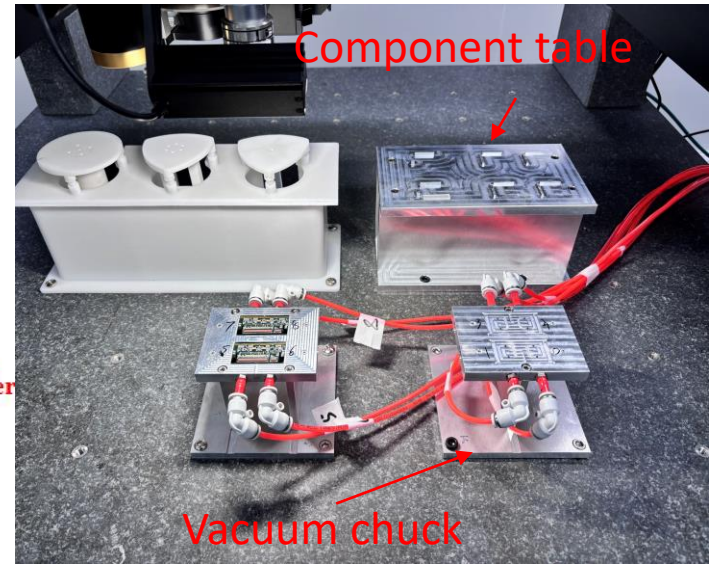
- The sensor will be flip-chip bonded to the ASIC, forming a hybrid, which is provided by IHEP for all of our hybrids.
- Two hybrids will be glued to a module flex PCB and wire bonded to create what we call a ‘Full Module’.
- A module assembled with only ASICs is referred to as a ‘digital module’.

	Type	Sensor	Metrology	WB	IV test	Vth tuning and Charge scan	Bonding check
DM001	Digital		OK	USTC		OK	
FM001	Full Module	IHEP IME (W24 11+W23 10)	OK	USTC	Broken		
FM002	Full Module	IHEP IME (W24 11+W23 10)	OK	USTC	OK	OK	Done
FM003	Full Module	IHEP IME (W24 19+W23 25)	OK	USTC	OK	OK	Done

Module assembly

Hardware for assembly

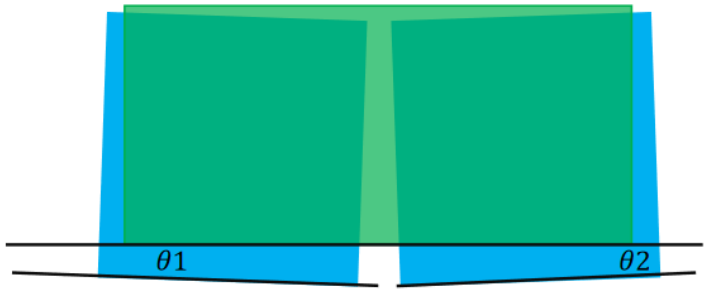


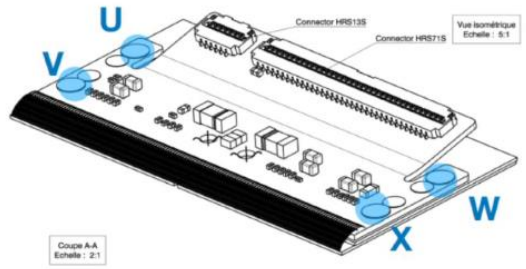


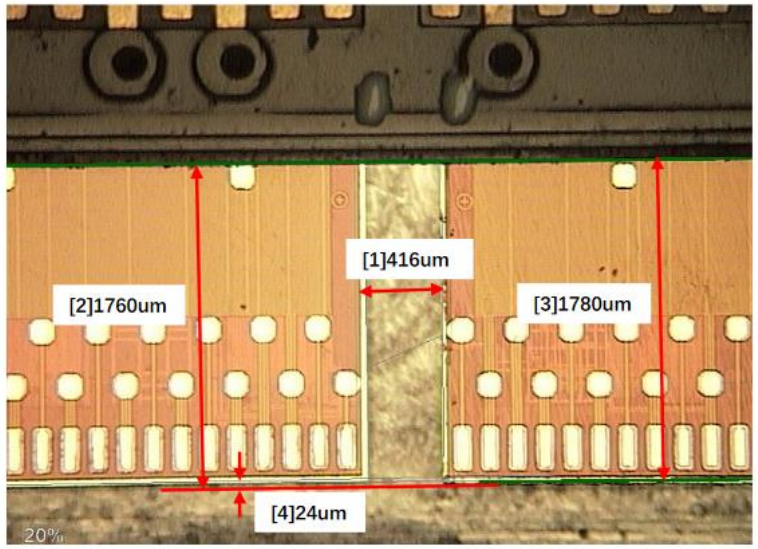
Hardware	Function
Gantry System	Place all component precisely
Glue dispense	Dispense glue automatically
Custom tools	Pick-and-place hybrid, PCB, glue
SmartScope	Metrology measurement

- A C# program was developed to control the gantry system at USTC. This software controls all the gantry system hardware.
- Once the components' position are set and the dispensing is calibrated, the assembly process will be completed automatically.
- With the new chuck, we can assemble four modules in parallel.

Metrology



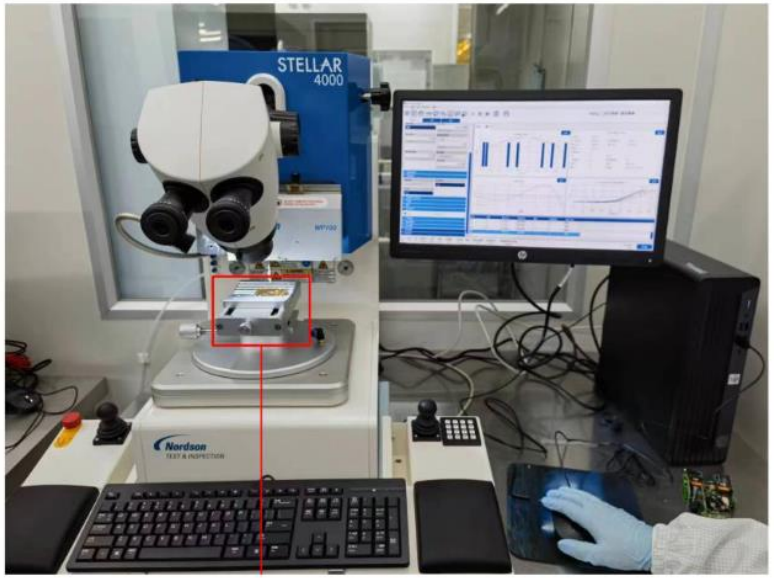




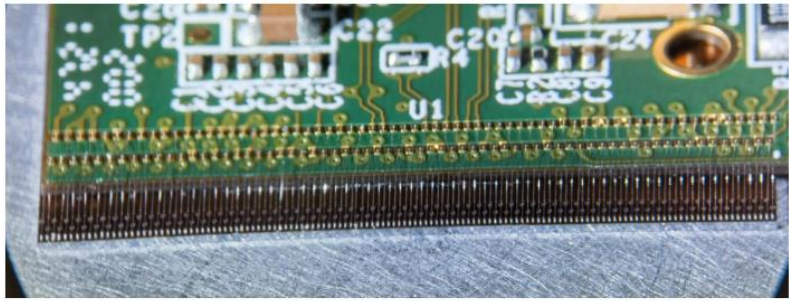
	Gap	D_{left}	D_{right}	U	V	X	W	$\theta 1$	$\theta 2$
Specification	400 ± 100 μm	1719 ± 100 μm		1.780 ± 0.075 mm				$< 0.1°$	
Test result	440	1660	1682	1.80	1.74	1.70	1.74	0.04	0.02

- The thickness of module, the distance between edge of ASIC and PCB, the orientation of ASIC will be examined.
- The test result of FM001 fulfills the specification, except the thickness of X.
- For the other module, after adjusting the vacuum chunk, all specifications are fulfilled.

Wire-bonding and Pull Strength test



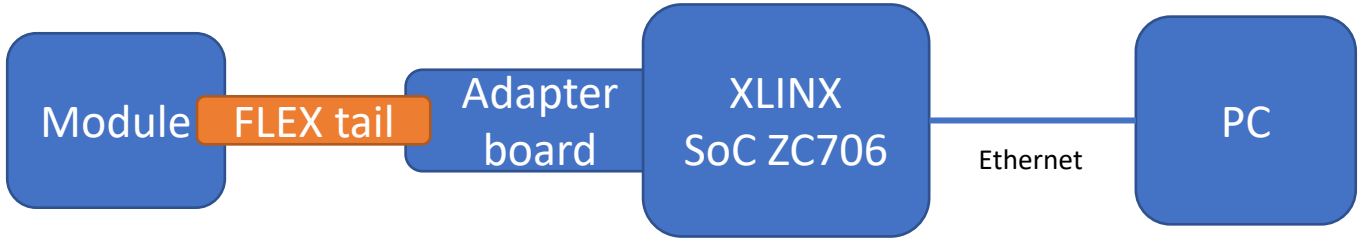
	Specification	Measured
Average	> 8g	8.67g
minimum	> 5g	7.63g

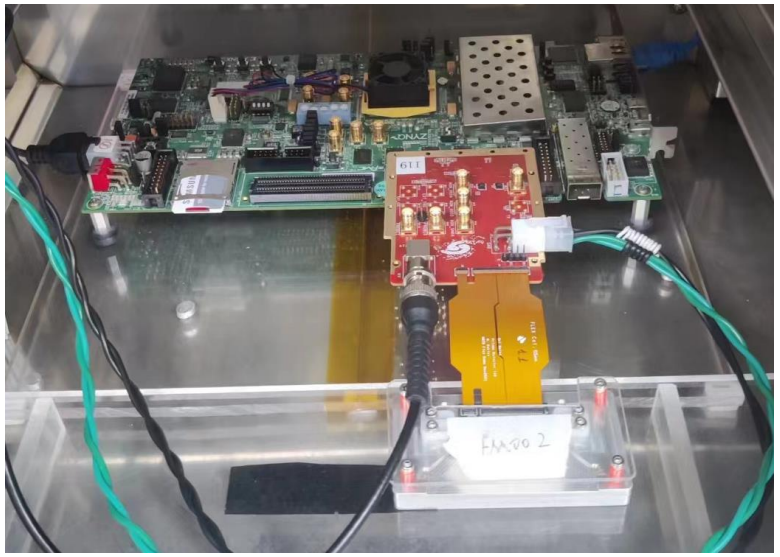


- The wire bonder BJ855 can automatically complete wire bonding after programming.
- Stellar 4000 bond-tester is used for pull test, the specifications are fulfilled.

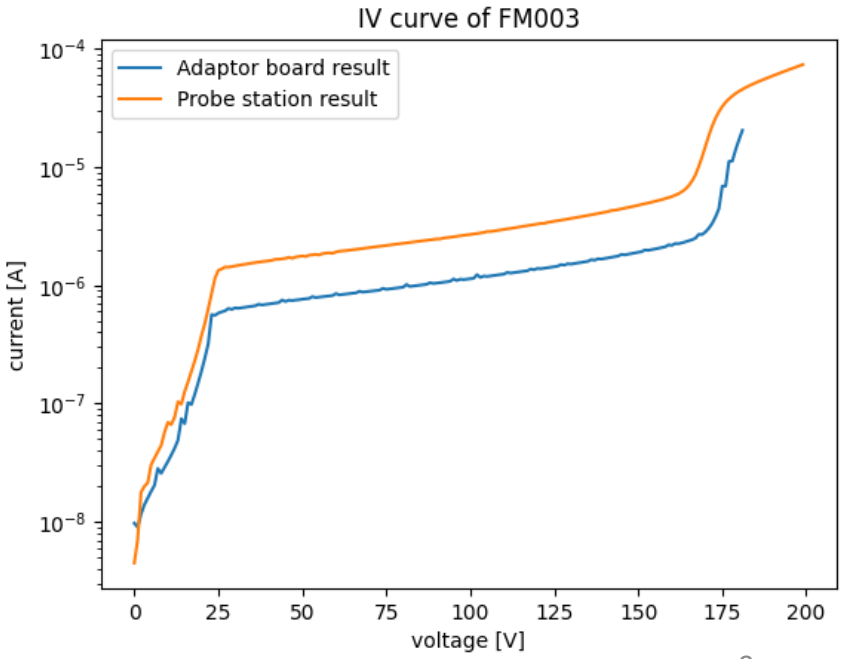
Electronics Test

Experiment setup and IV check

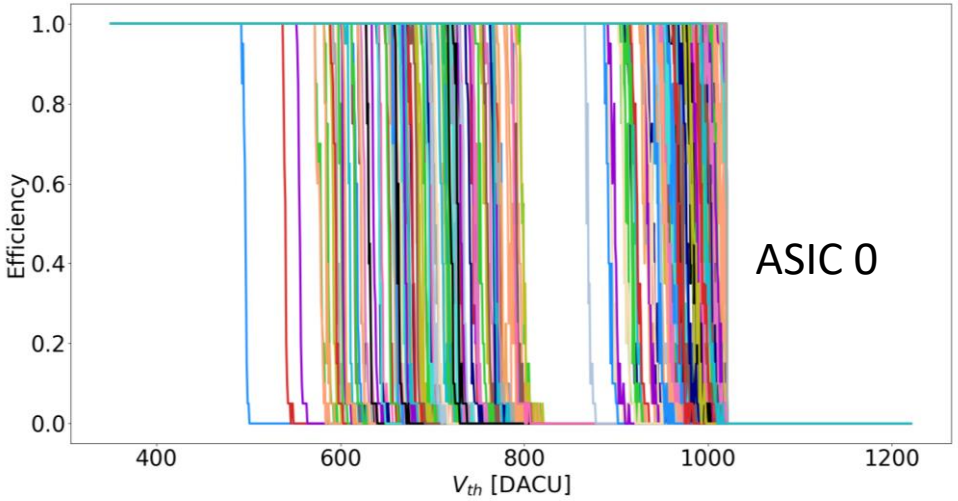


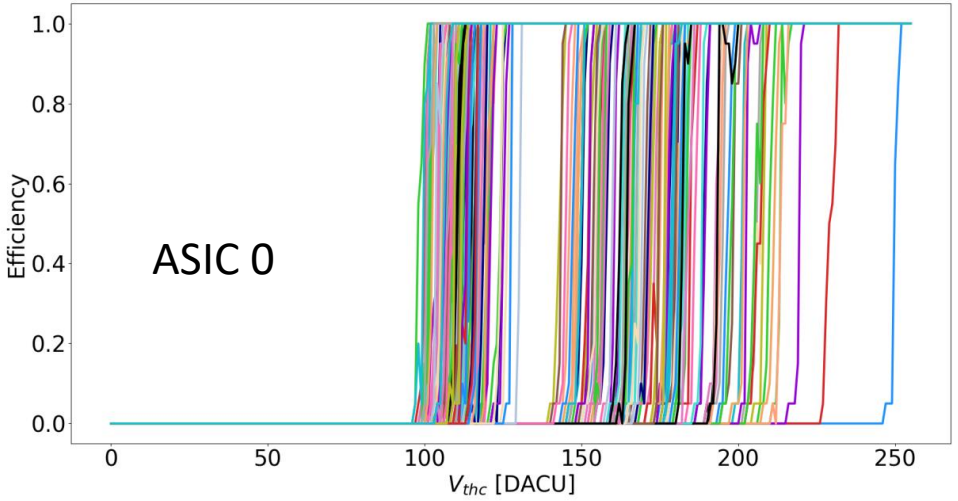


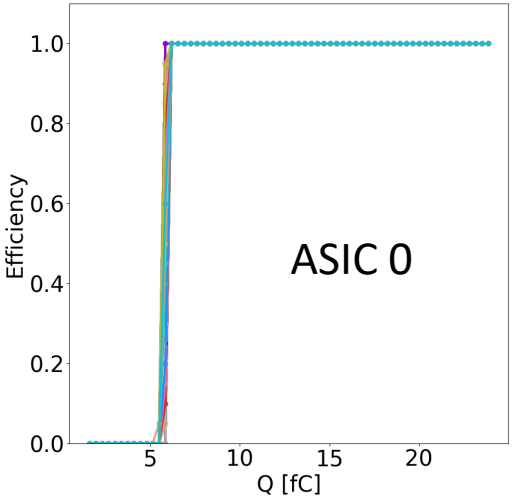
- Using adaptor board provided by IHEP and SDU, which provides power, clock, data transfer to the ASIC, and high voltage to the sensor.
- Using ZC706 and FADA as readout system. Scripts for testing and analysis have been migrated from the FADA repository.
- Climate chamber are used to
  - shield the light from outside.
  - maintain the temperature at 20 °C, consistent with the probe station.
- The results obtained from the module test system are comparable to those from the probe station, with slightly lower current after depletion.



Threshold voltage and Charge scan

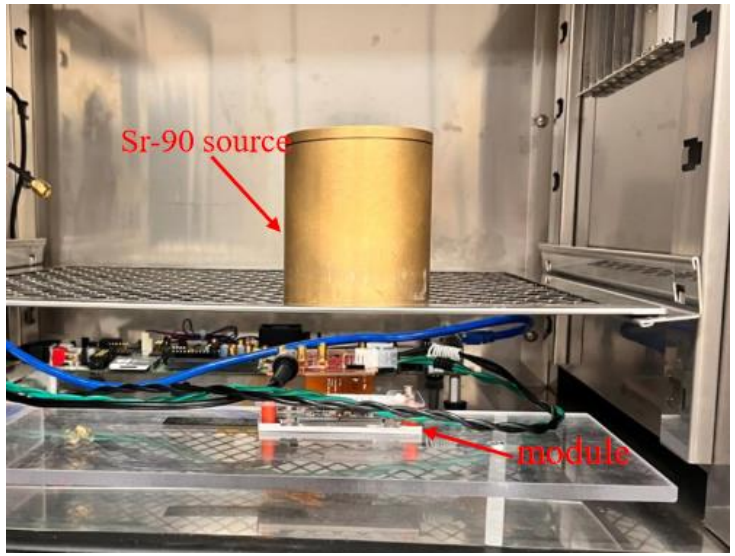


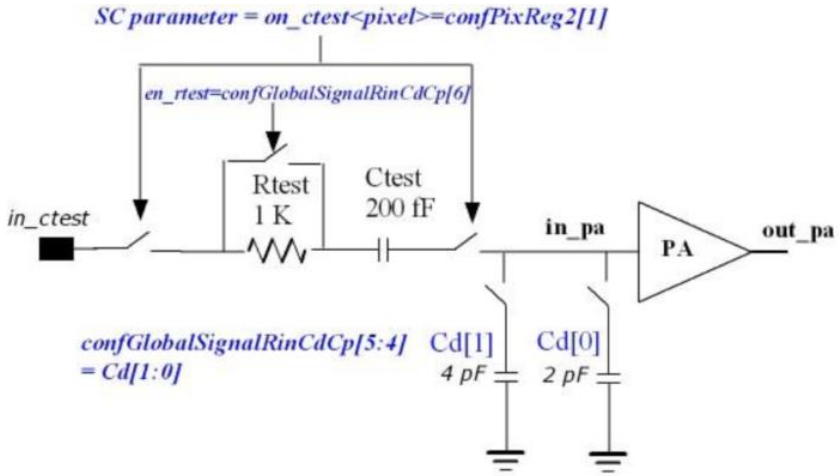




- The injected charge is set to 12 DACU, equivalent to approximately 4.8fC.
- As the code value of Vth increase, the threshold voltage increase, the efficiency decrease.
- With the increase of the Vthc code value, the threshold voltage gets lower and the efficiency increases.
- The threshold voltage corresponds to 50% efficiency point. The median of Vth scanning result is chosen as global threshold voltage.
- The charge scan shows that the Vth is well-tuned, and the results meet our expectations.

Radioactive source test





- For the full module, check for the bump bonding between sensor and ASIC is necessary.
- A radioactive source can be used to check this.

Electron induce signal → Random trigger sent to ASIC → Coincidence count will be output

- Experiment setup:
  - DUT: Full modules
  - HV: -150V
  - Temperature: 20 °C
  - Radioactive Source: Sr-90
  - All channels are turned on
  - DAC Charge is set to 0
  - Ctest is disabled for all channels
  - No calibration command sent

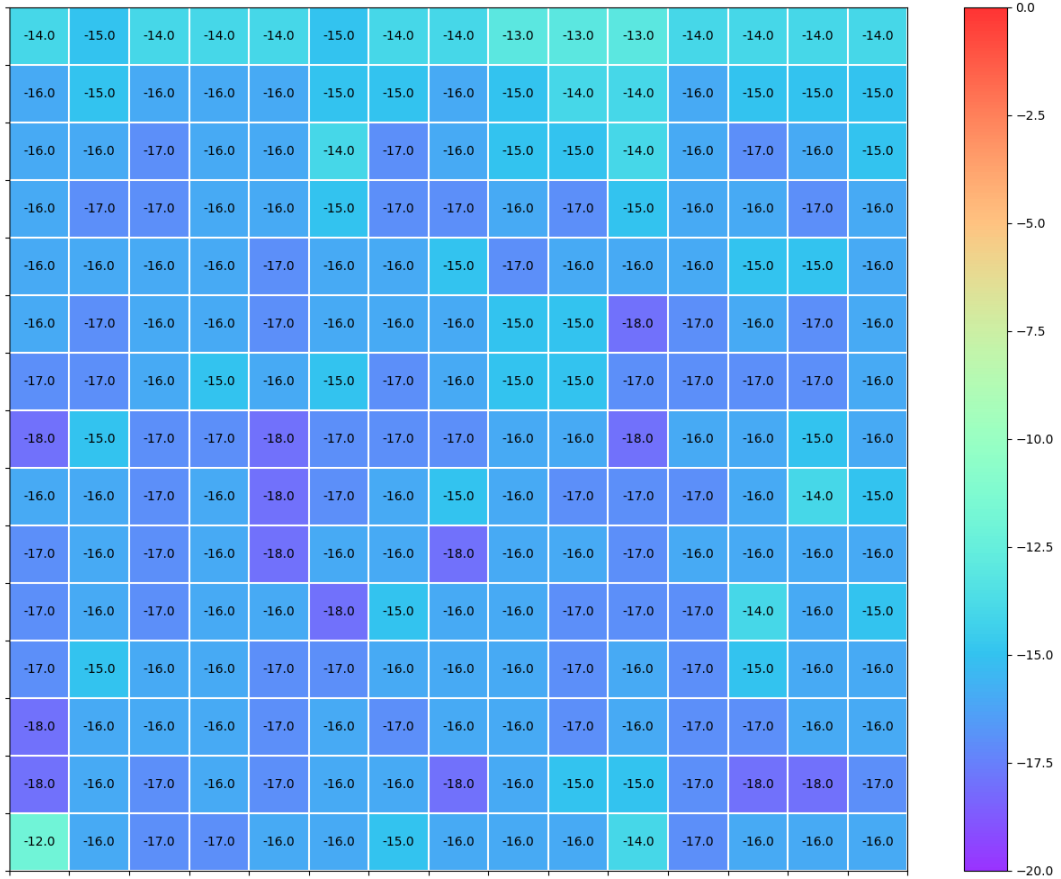
Bonding check with Vth scan

- The capacitance of detector varied with the bias voltage, which can be used to check the bump-bonding.

Capacitance decrease → Signal amplitude increase → Threshold voltage increase

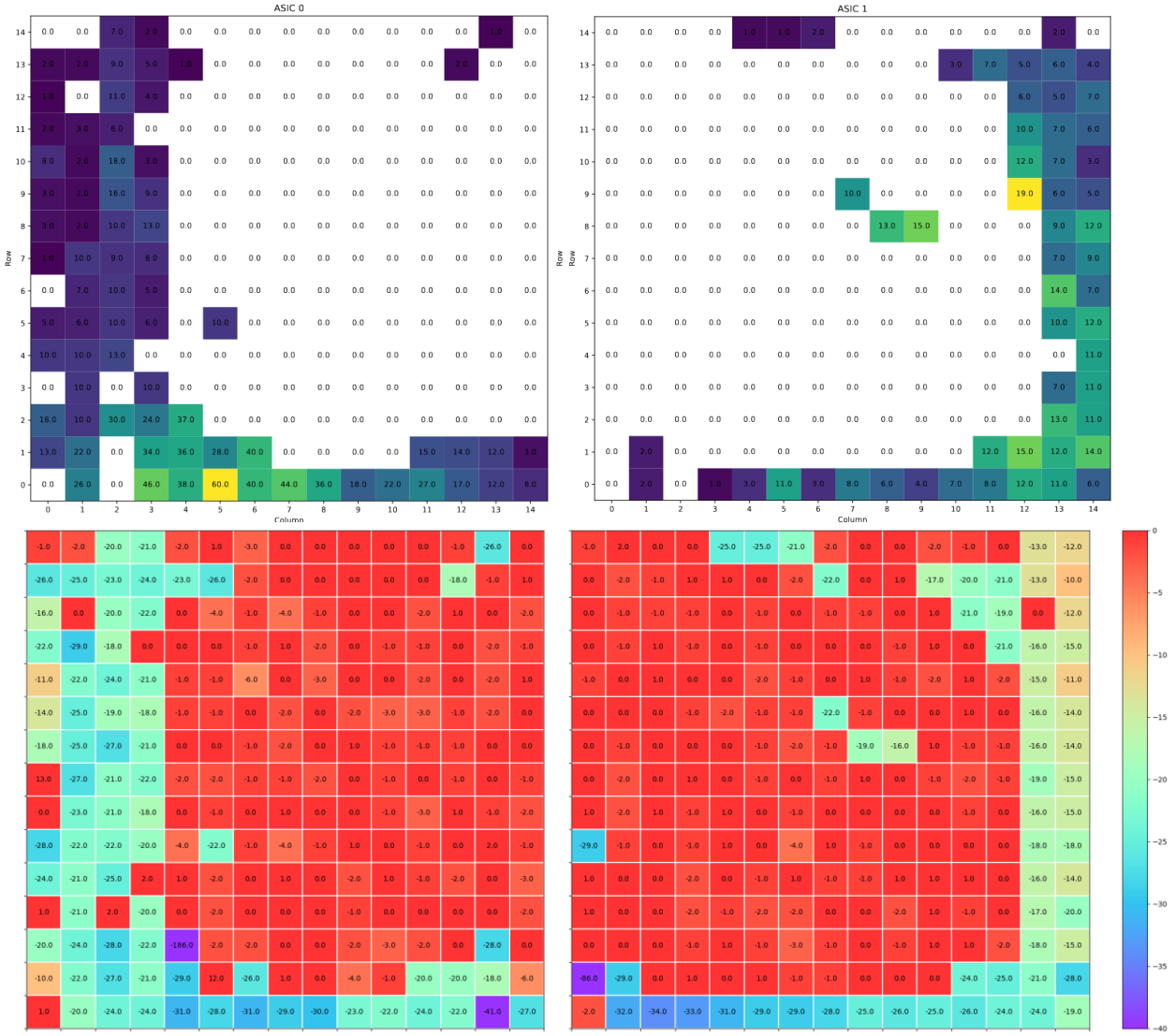
- We perform Vth scan with different capacitance (1pF -> 3pF) set using Altiroc3 to validate this method.
- The injected charge is set to about 5fC.
- For LGAD sensor, the capacitance changes from 400pF to 4pF with HV-off to depleted.
- This method could be used to check connection.

Vth variation



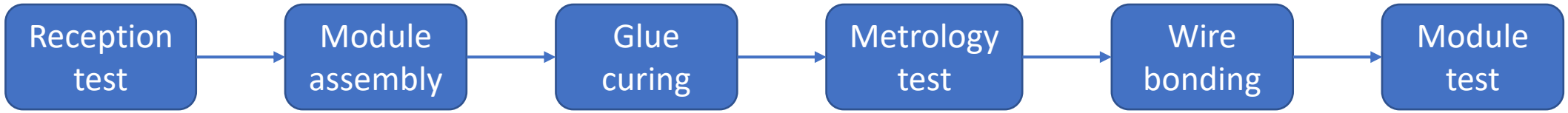
Bump Bonding Check

FM003



- For radioactive source measurement. Vthc is tuned with 4.8fC charge injection.
- Because Vthc is tuned with a relatively high charge injection, noise-induced hits are minimal.
- The absence of hits in some channels may be due to their greater distance from the center of the radioactive source.
- We have also obtained comparable results using two methods.
- Most of the channels of sensor are not connected to the ASIC.
- The ACP technique for flip chip bonding has been attempted and shows higher reliability; more details can be found on my poster.

Summary and plan



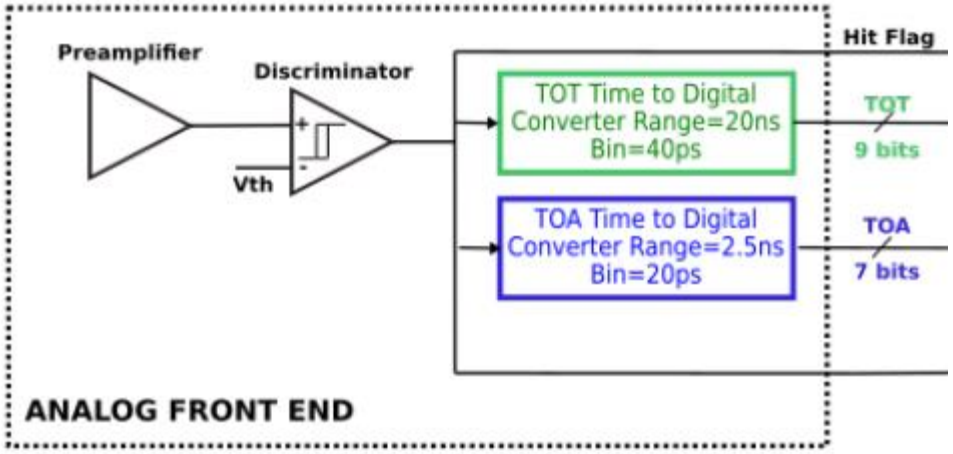
- We have established a system for module assembly, encompassing gluing and wire bonding.
- Additionally, a module testing system has been set up at USTC, covering metrology, pull tests, and electronics testing.
- We have successfully produced one digital module and three full modules.

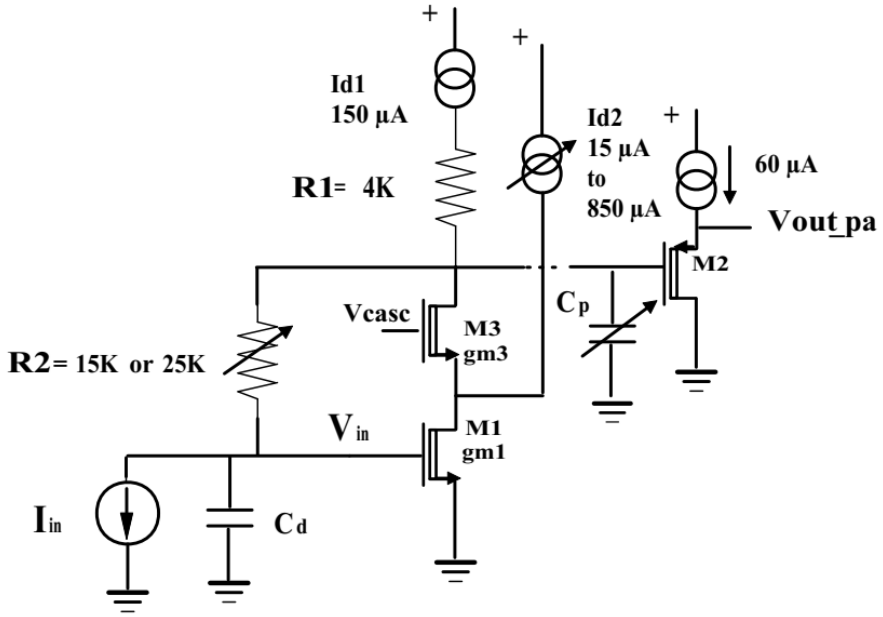
- Try to improve production process and adjust equipment to achieve target assembly rate.
- Get ready for the production of HGTD.

Thanks for your attention!

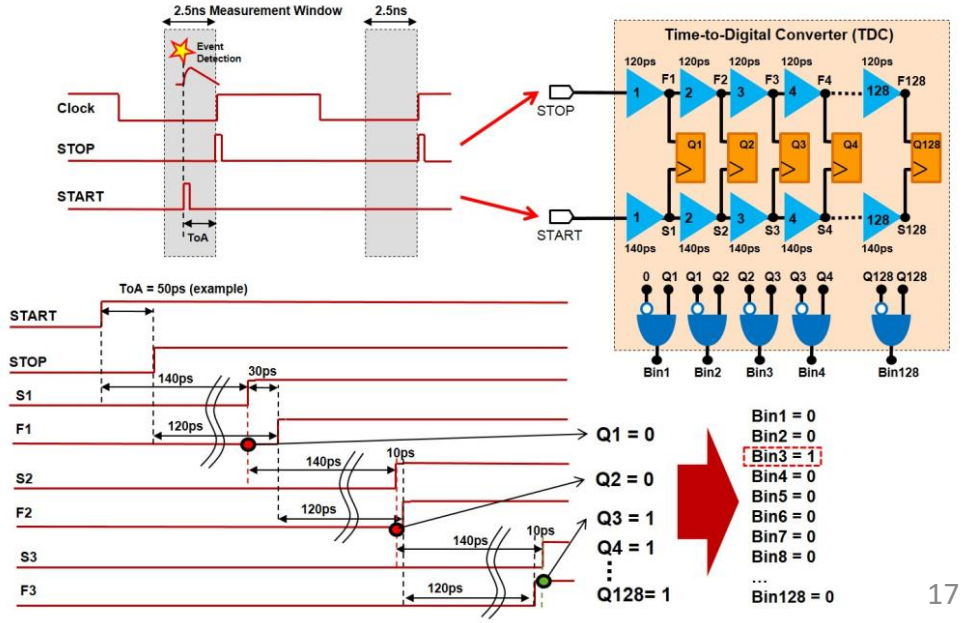
Backup

Analog front end

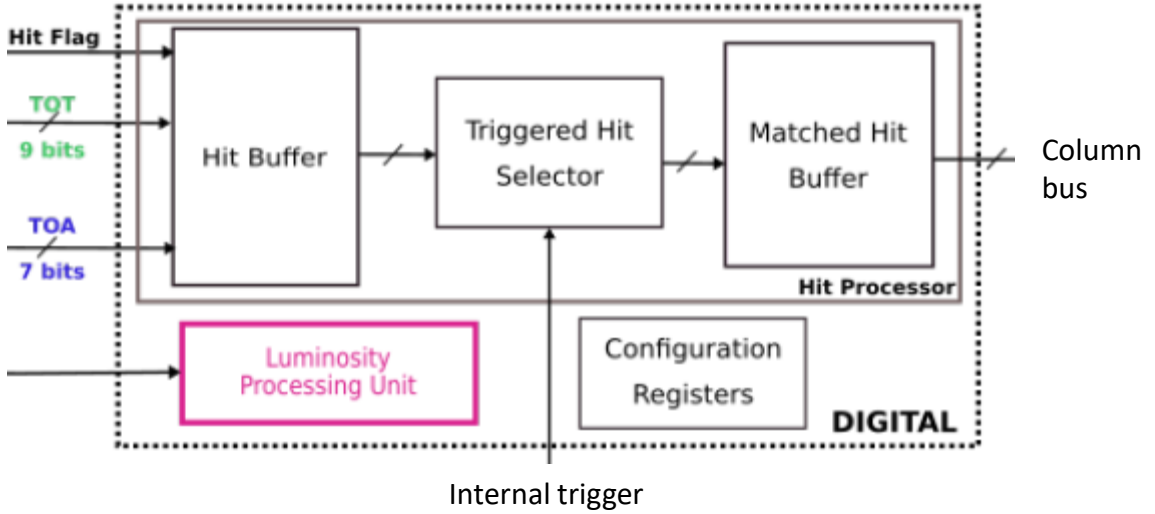




- The design of the preamplifier uses a voltage sensitive preamplifier.
- The discriminator is built about a high speed leading edge architecture with hysteresis.
- The TDC employs Vernier delay line configuration.



Hit Processor



Writing Pointer, +1 for each bunch cross.

Reading Pointer, when THS receives trigger, it will be handled by THS.

Hit Buffer

TOA	TOT	Hit flag	TOA overflow	CRC
7 bits	9 bits	1 bit	1 bit	2bit
. . .				
7 bits	9 bits	1 bit	1 bit	2 bit

Matched Hit Buffer

Time information	TrigID
16 bits	5 bits
. . .	
16 bit	5 bits

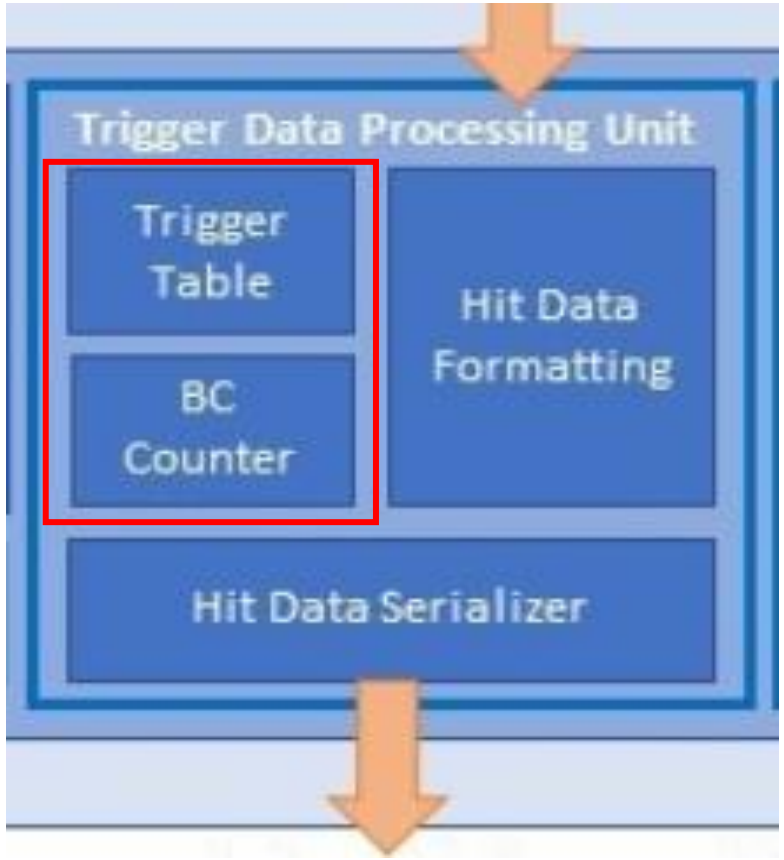
There will be 1400 positions corresponding to 35 μs latency for L_1 trigger.

Triggered Hit Selector

Internal trigger

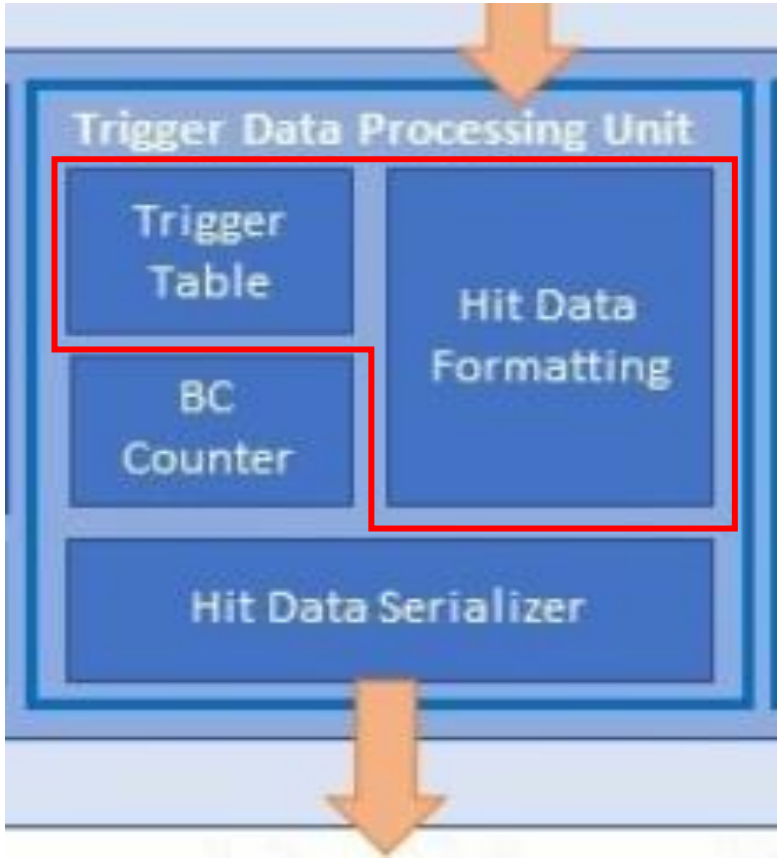
The current design has a depth of 32.

Trigger and TrigID



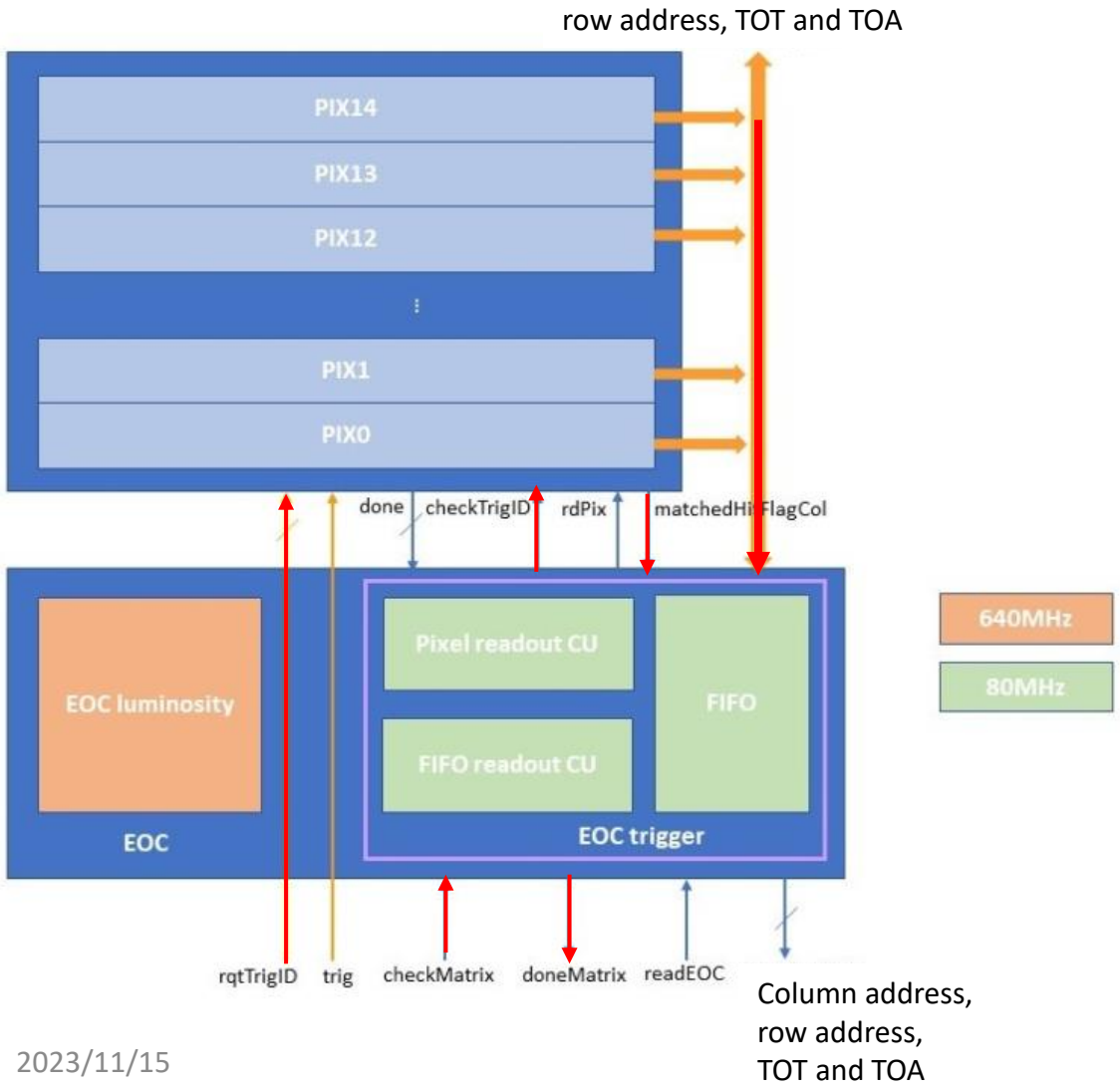
- When the TDPU receives a trigger command, it stores the content of the counter (TrigID) together with the corresponding BCID into the trigger table and increases the counter by one unit.
- The TDPU unit also generates an internal trigger signal with a duration of one clock cycle. This is immediately transmitted to all matrix channels as well as the TrigID.

Data transmission: Initiation



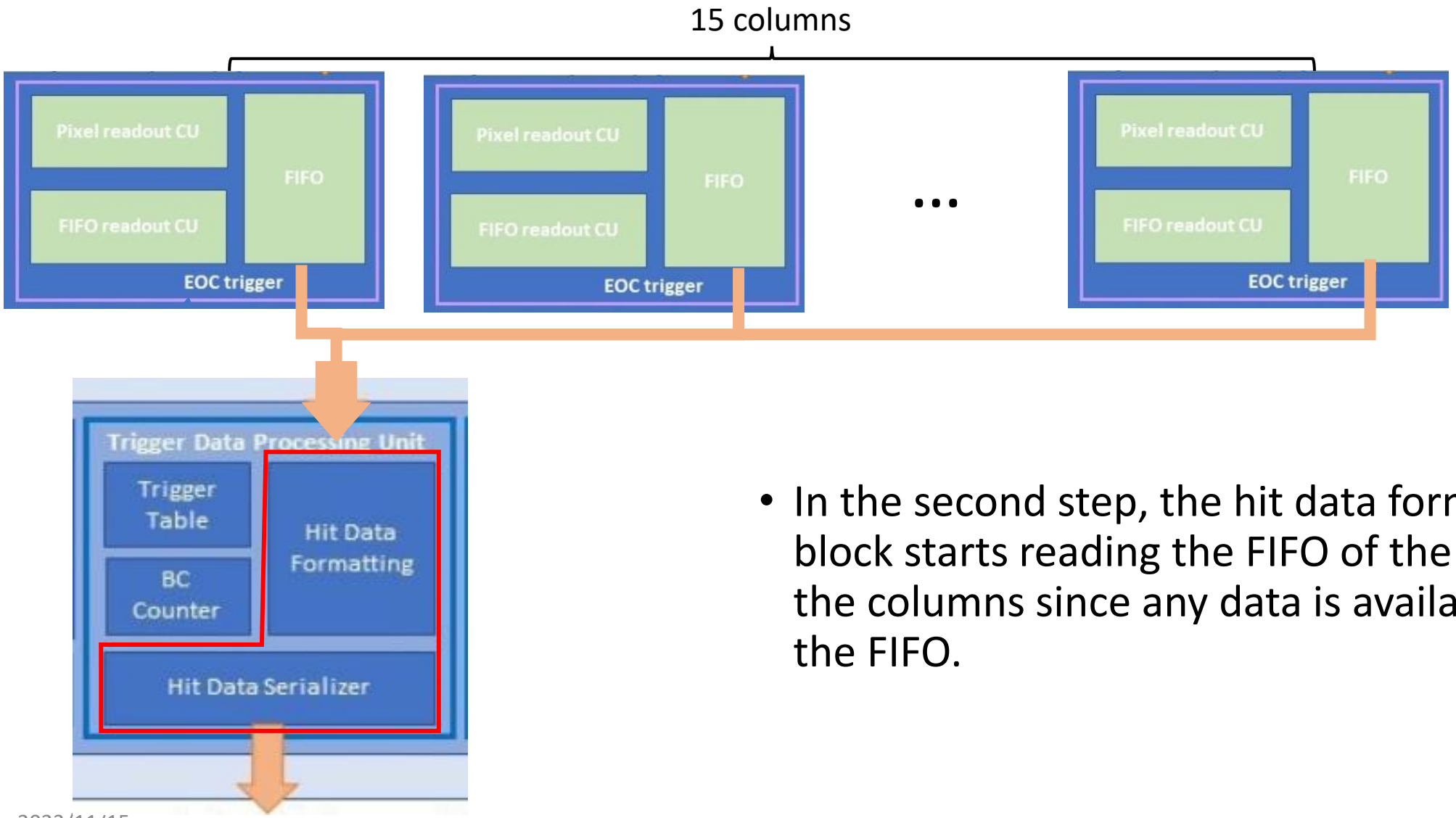
- The hit data formatting unit continuously checks the trigger table. When one is found, it fetches the entry and initiates the readout of the data.
- The hit data formatting unit places the *TrigID* in the *rqtTrigID* bus and send *checkmatrix* signal.

Data transmission: EOC blocks



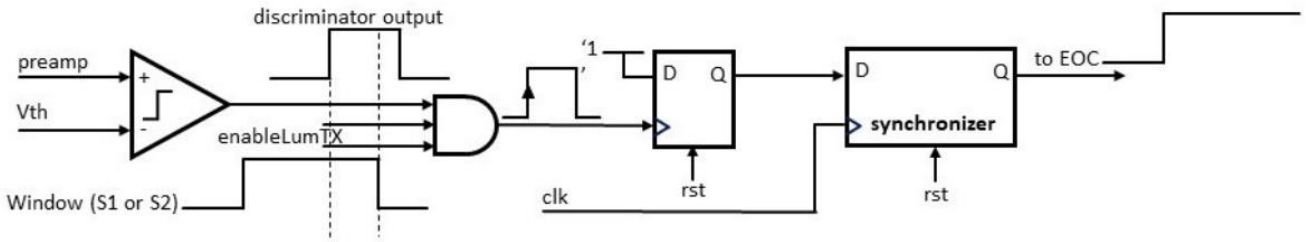
- The readout is carried out in two steps.
- First step is the retrieval of data associated to a given TrigID from the columns, and then the frame construction and data transmission.

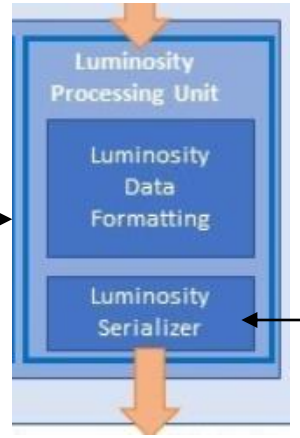
Data transmission: TDPU



- In the second step, the hit data formatting block starts reading the FIFO of the end of the columns since any data is available in the FIFO.

Luminosity





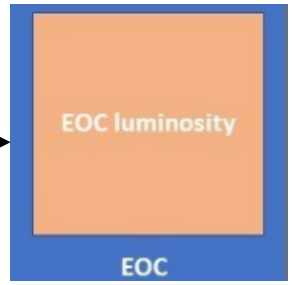
Single channel windowing process

EOC sums the measurements of whole column

sums the measurements of the columns

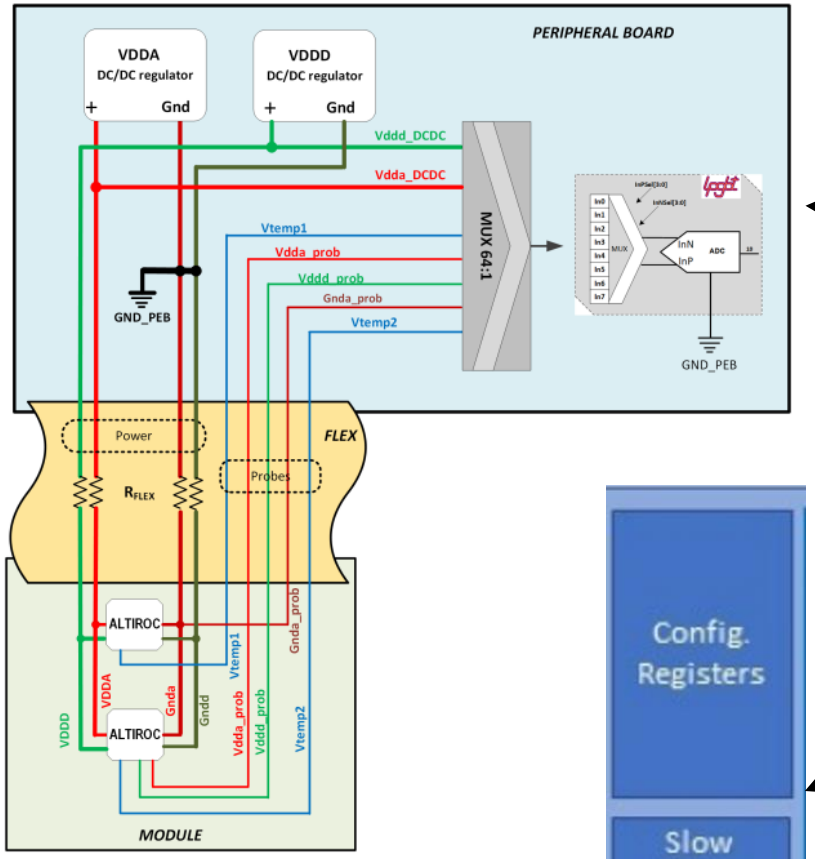
S2-S1 and S1 are truncated to 5 and 7 bits

encoded with 6b8b code, 16-bit frame



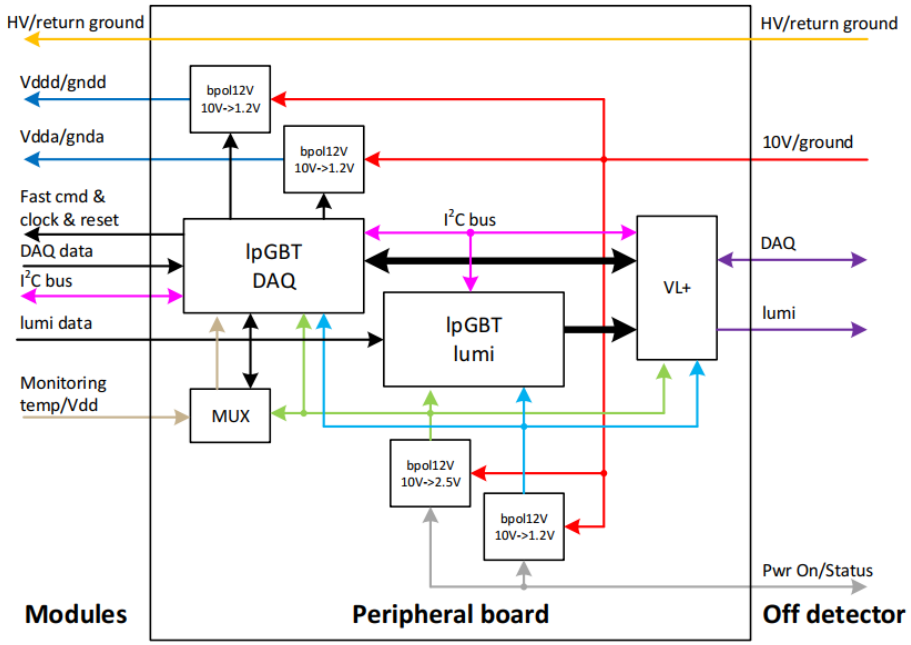
- The two windows are generated at the EOC and distributed to the whole column as a clock tree in order minimize the skew from pixel to pixel.

Monitoring and Configuration



- Three signals (Vdda_prob, Vddd_prob and Gnda_prob) for the monitoring of the power supply voltages and two signals (Vtemp1, Vtemp2) for the measurement of the temperature are connected to the ADC of the lpGBT.
- In order to configure the ASIC as well as to retrieve information of its internal status, 1024 configuration registers of 8-bits each have been implemented in ALTIROC. The configuration registers are read/written by using an I^2C link.

PEB



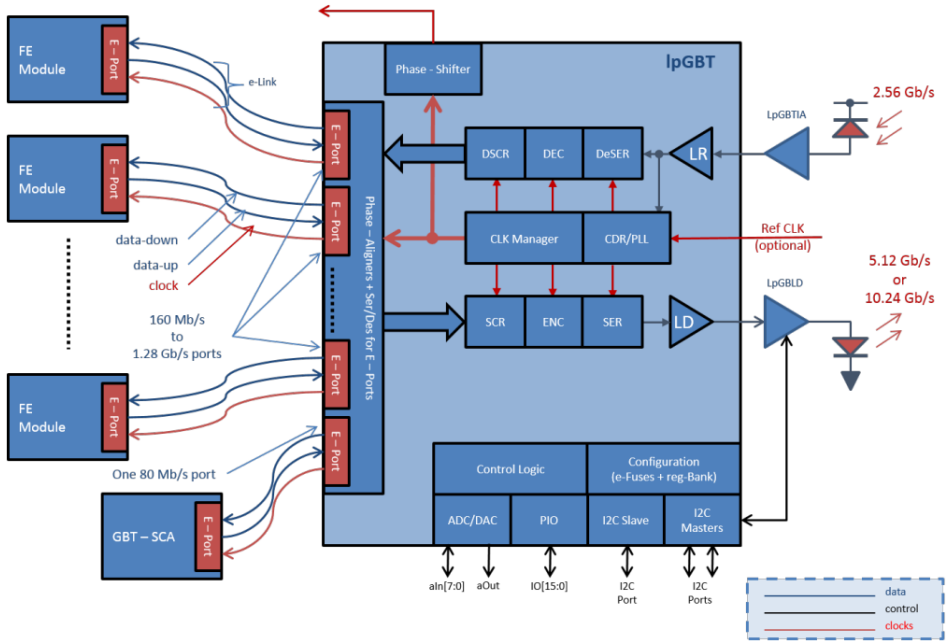
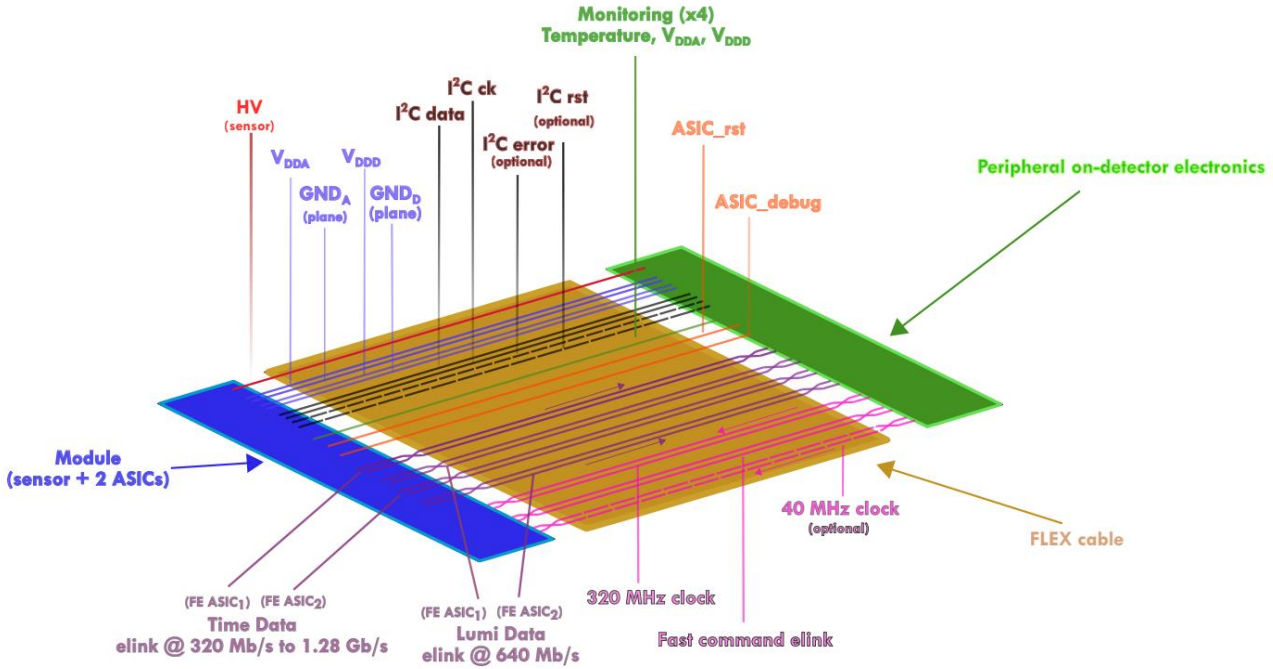
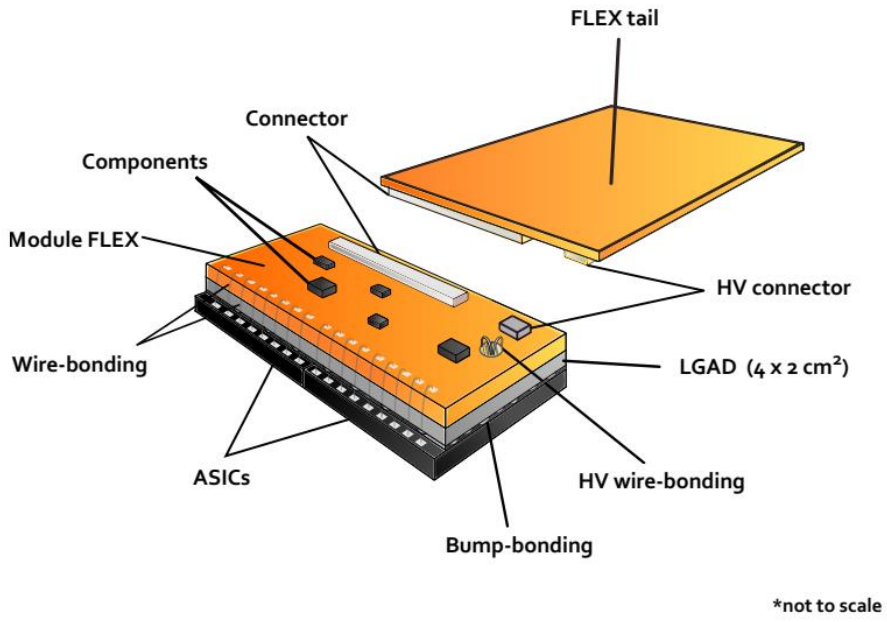


Figure 9.6: Block diagram of the lpGBT ASIC.

- The main chip for data transmission on PEB is low-power GigaBit Transmission chip (lpGBT).
- lpGBT will extract and distribute 320 MHz clock, fast command to ALTIROC. Different lpGBT will be used to collect time data and luminosity data from ALTIROC.
- Configuration information for ALTIROC and lpGBT used for luminosity data will be transmitted with I^2C buss.

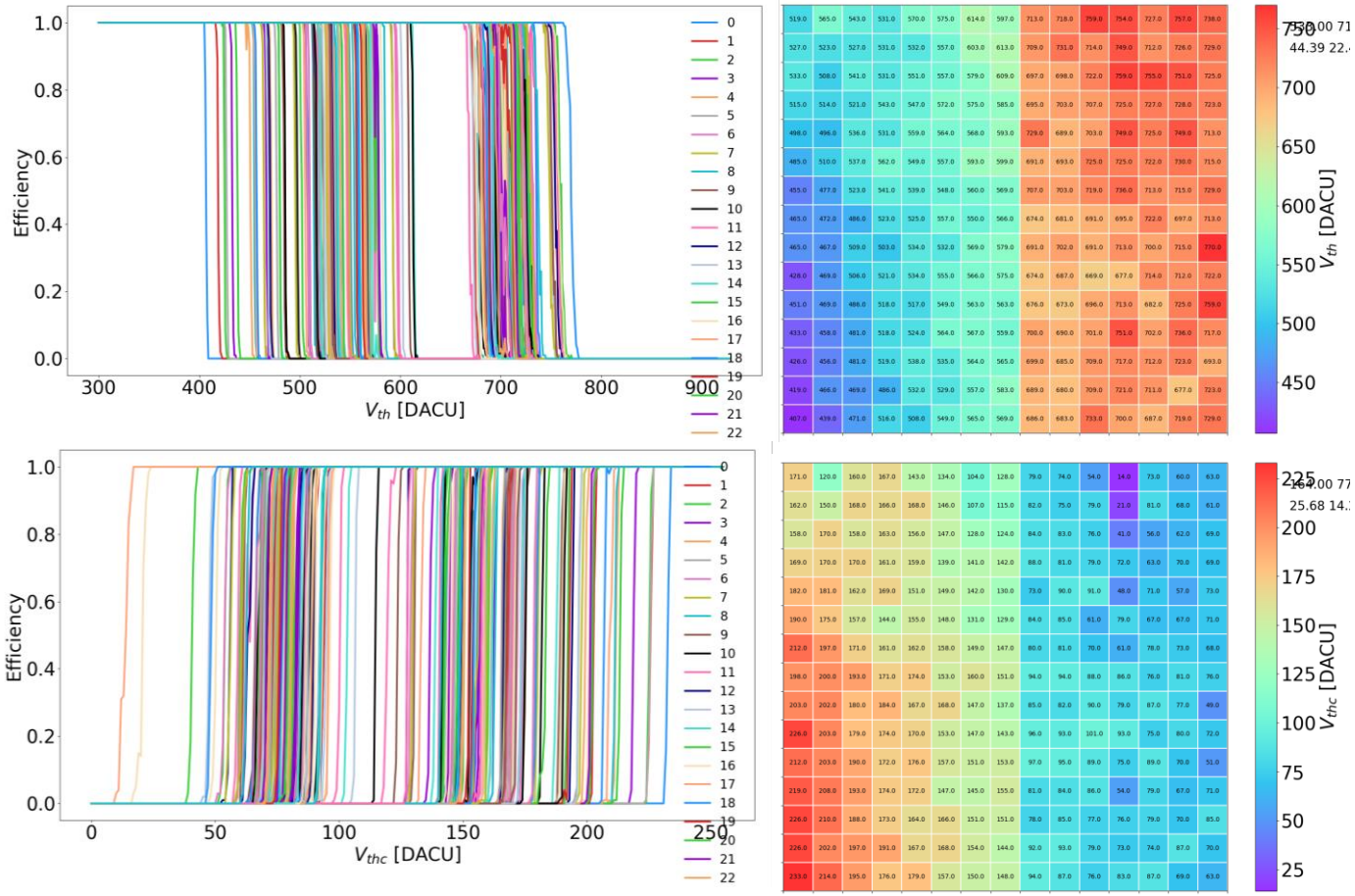
Connection





- The PEB and module FLEX are connected with flex cable.
- The sensor and front end ASIC are connected with bump-bonding.
- The ASIC and module FLEX are connected with wire-bonding. Wire-bonding is also used to provide HV for the sensor.

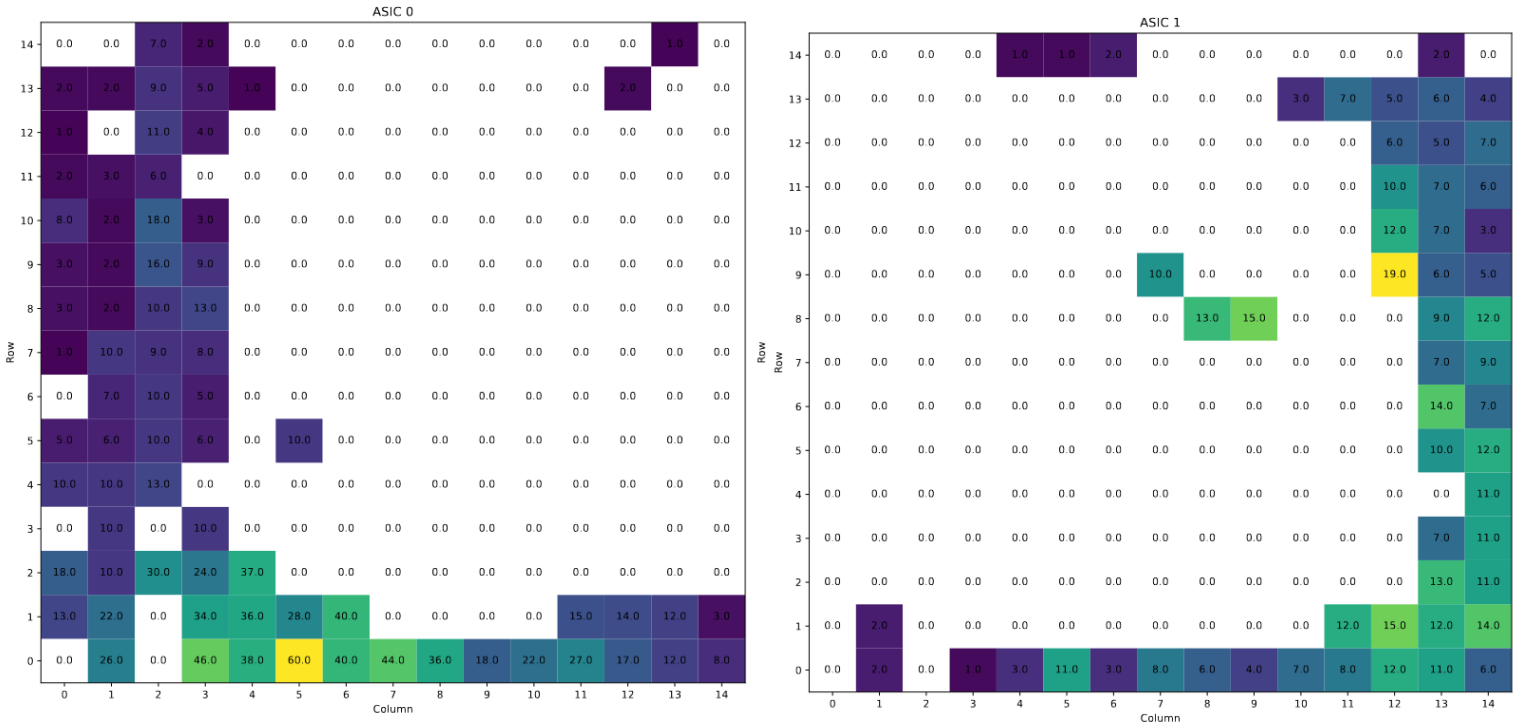
Vth scan

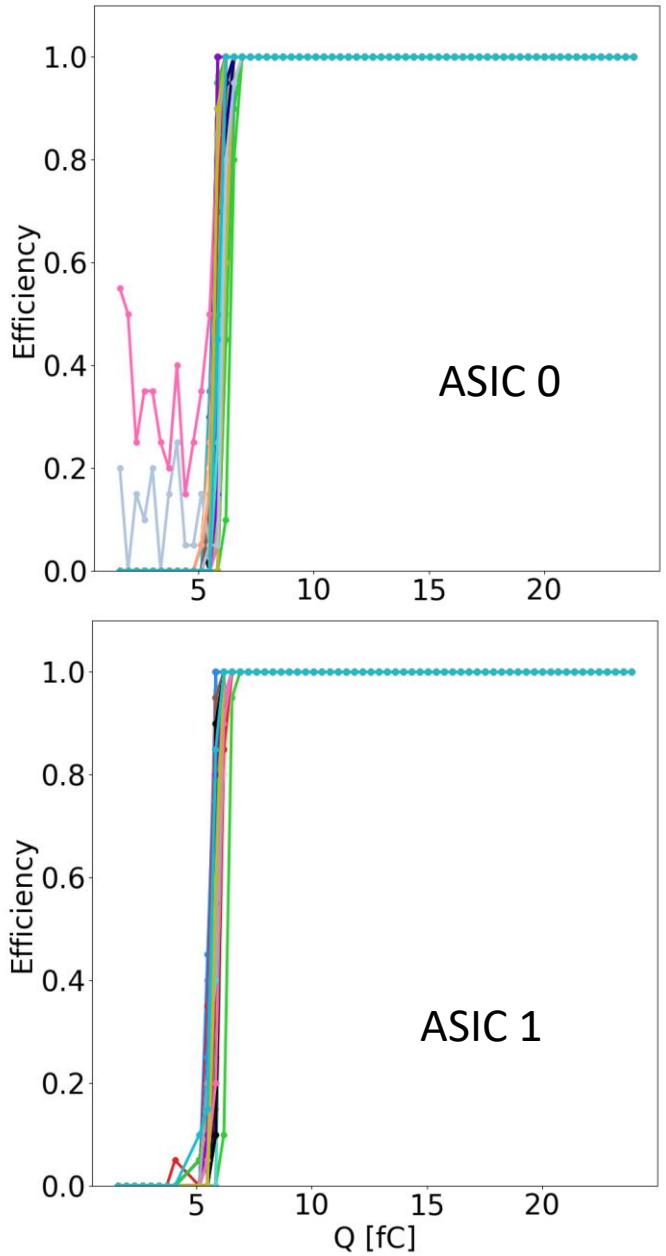


- Threshold voltage scanning is performed with 4fC charge injection.
- We extracted global threshold voltage (593 DACU ~ 976.15mV), which is median of the 50% efficiency points for all channels.
- The difference between left and right part is caused by different types of preamplifier: voltage preamp, trans-impedance preamp.
- We can extract proper threshold voltage configuration with this scanning.

FM003 Source scan

FM003

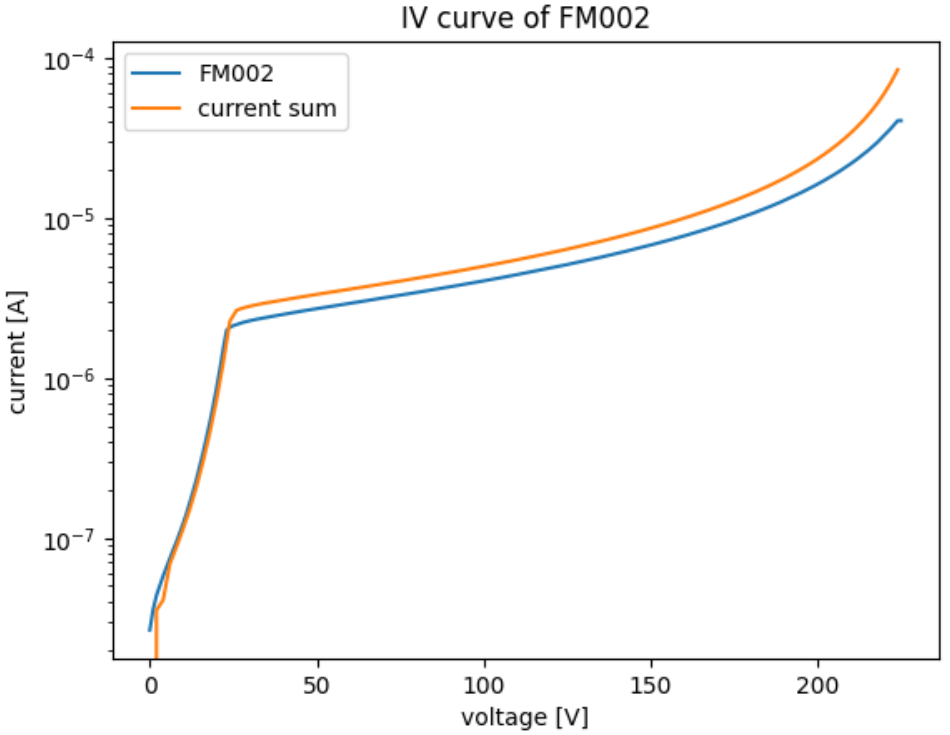


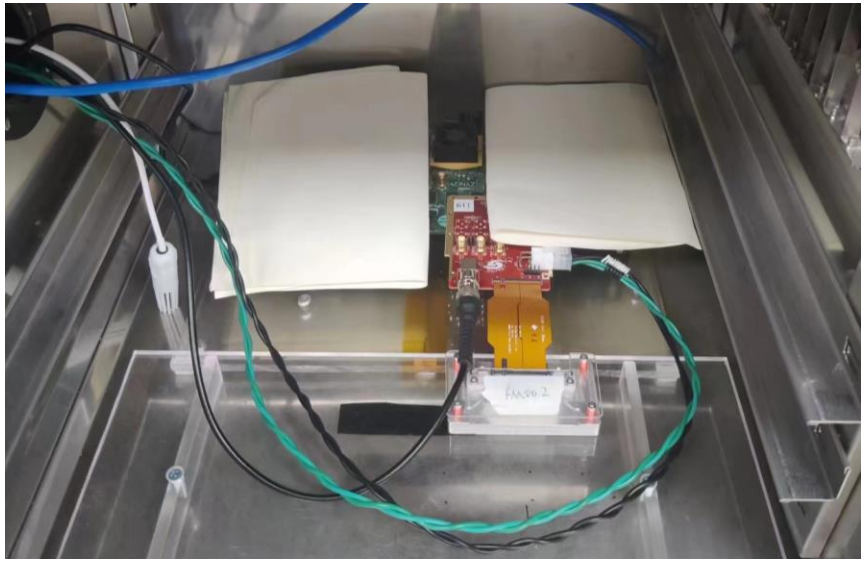


- The VTHC is tuned with 4.8fC charge injection.
- The data are merged from two tests: one targeting the radioactive source at ASIC0, and another centering at ASIC1.
- Most of the channels of sensor are not connected to the ASIC.

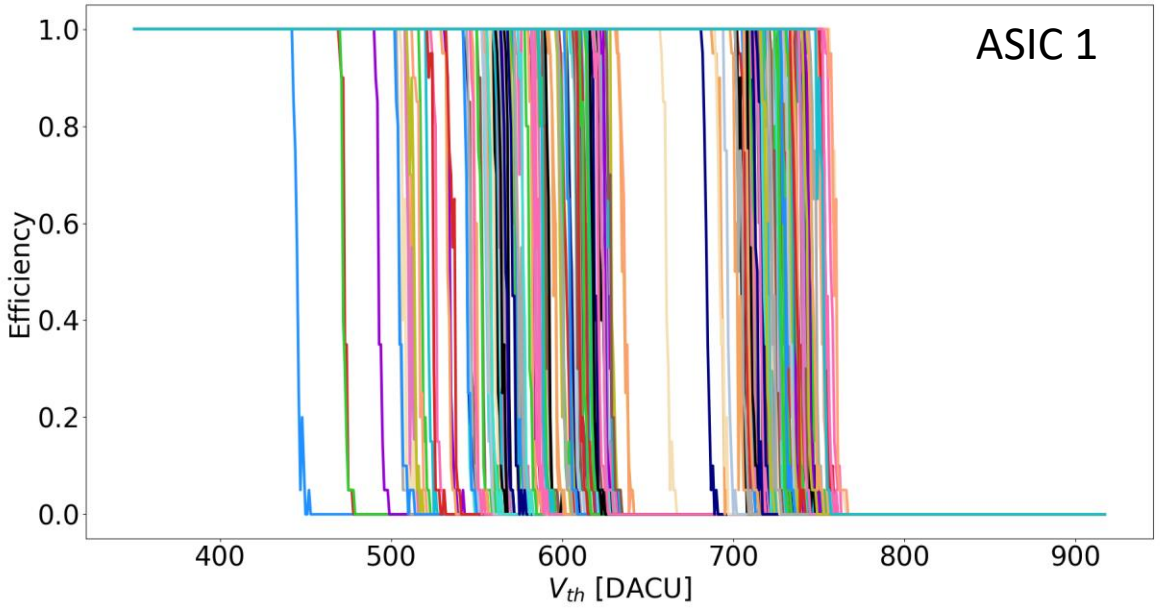
IV measurement

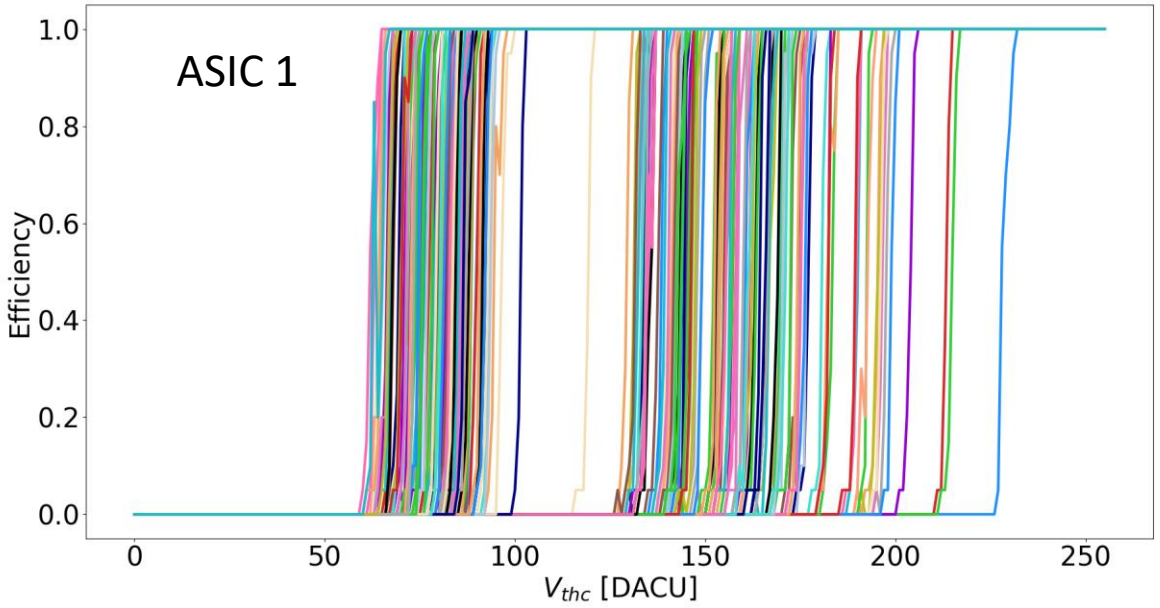
- For the Full Module, some additional checks need to be performed, including IV measurements and connection check between ASIC and sensor.
- Climate chamber are used to
  - Shield the light from outside
  - Keep the temperature at 20 °C, which is the same as probe station.
- The results obtained from the module test system are comparable to those from the probe station.
- After depletion, the current obtained from the module test system is slightly lower.





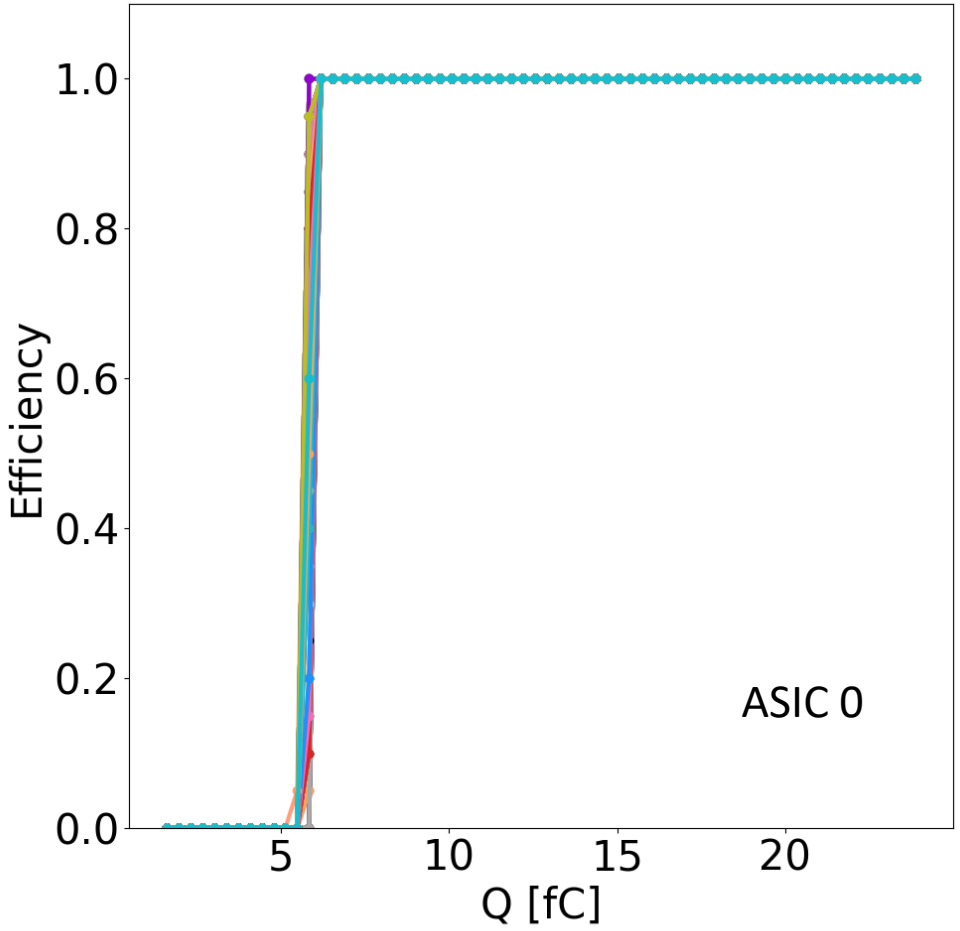
Channel threshold voltage

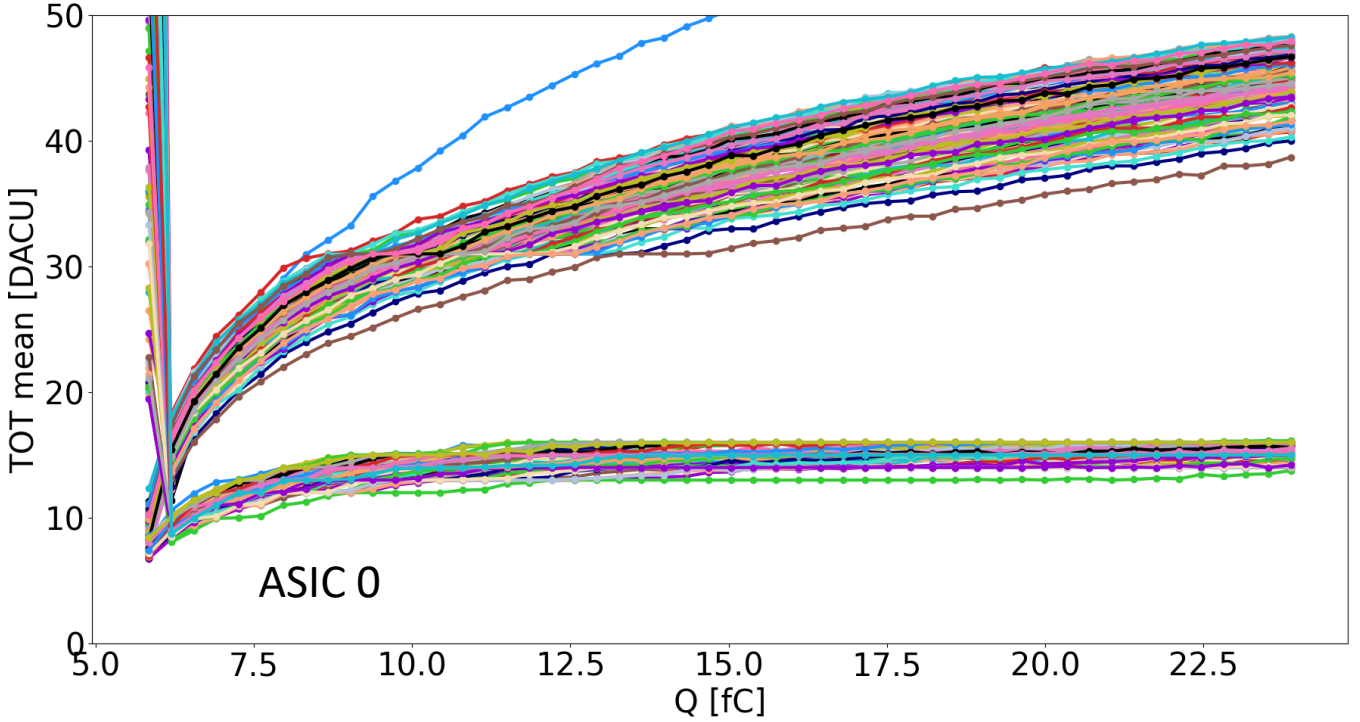




- The LSB of vthc is -1.04mV, with the increase of DACU, the threshold voltage gets lower and the efficiency increases.
- The 50% efficiency point will be recorded and used in charge scan.

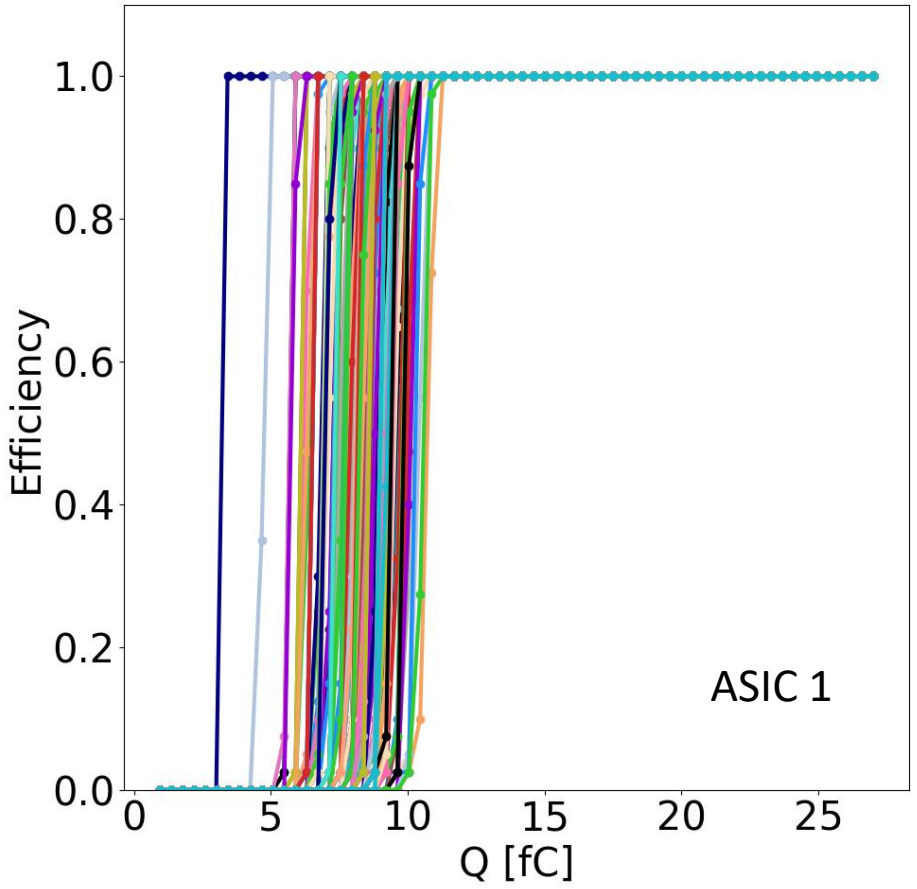
Charge scan

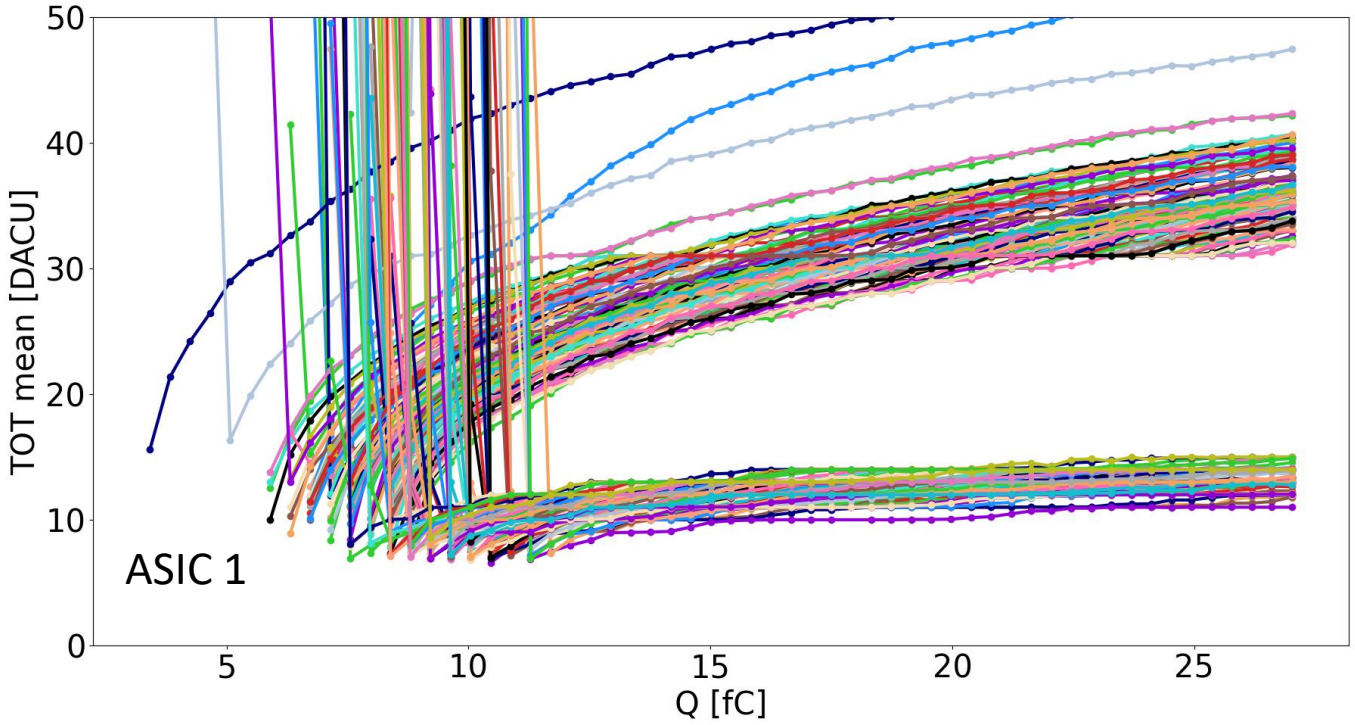




- The efficiency and TOT increase, with the increase of injected charge.
- The two different clusters in TOT is induced by preamplifier.
- The VTH is tuned very good, and the result meets our expectation.

Charge scan





- Same situation for ASIC1
- All required electronical measurement can be done at USTC site.

Assembly rate

- Current situation:
  - Reception test (20min/hybrid)
    - Hybrid IV measurement on probe
  - Module assembly (20min/module)
    - Prepare components and calibrate position (10min/module)
    - Automated assembly (10min/module)
  - Glue curing (7hr/module)
  - Metrology (30min/module)
  - Wire-bonding (~1hr/module → a few min/module)
    - The automation of the wire bonder has not been realized and occasionally needs to rewire missing pads by hand, resulting in unstable wire-bonding time
    - In principle it should be very quick with our auto wire bonder (a few min)
  - Module test(~1hr/module)
    - Assume no issue during test (Vth, Vthc, Charge scan) ~ 1 hour per module
    - Need longer time if radioactive source scan and thermal cycling are performed
- Target rate: 4 modules per day