High Granularity Timing Detector activities at IHEP/NJU

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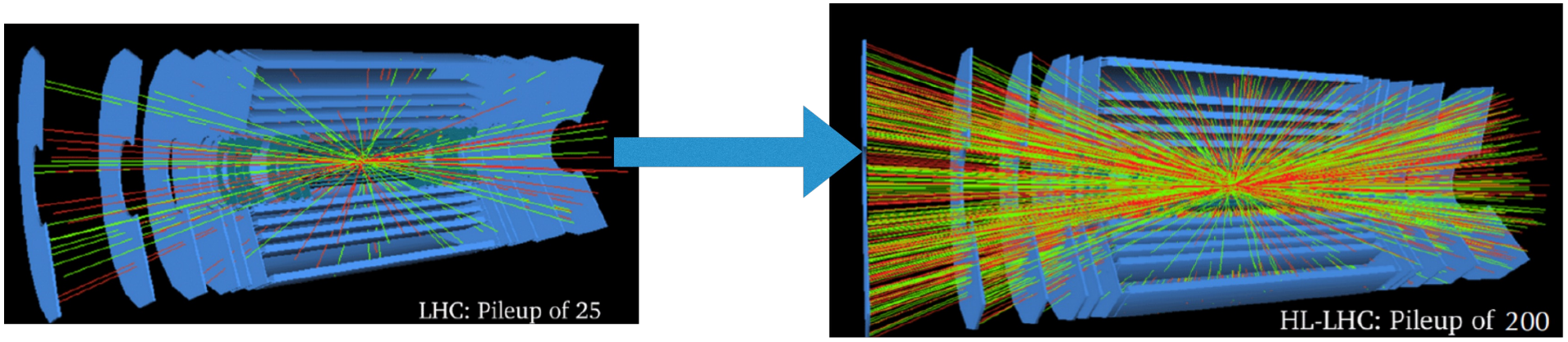
On behalf of IHEP/NJU HGTD team

The High-Luminosity-LHC Challenges to Detectors

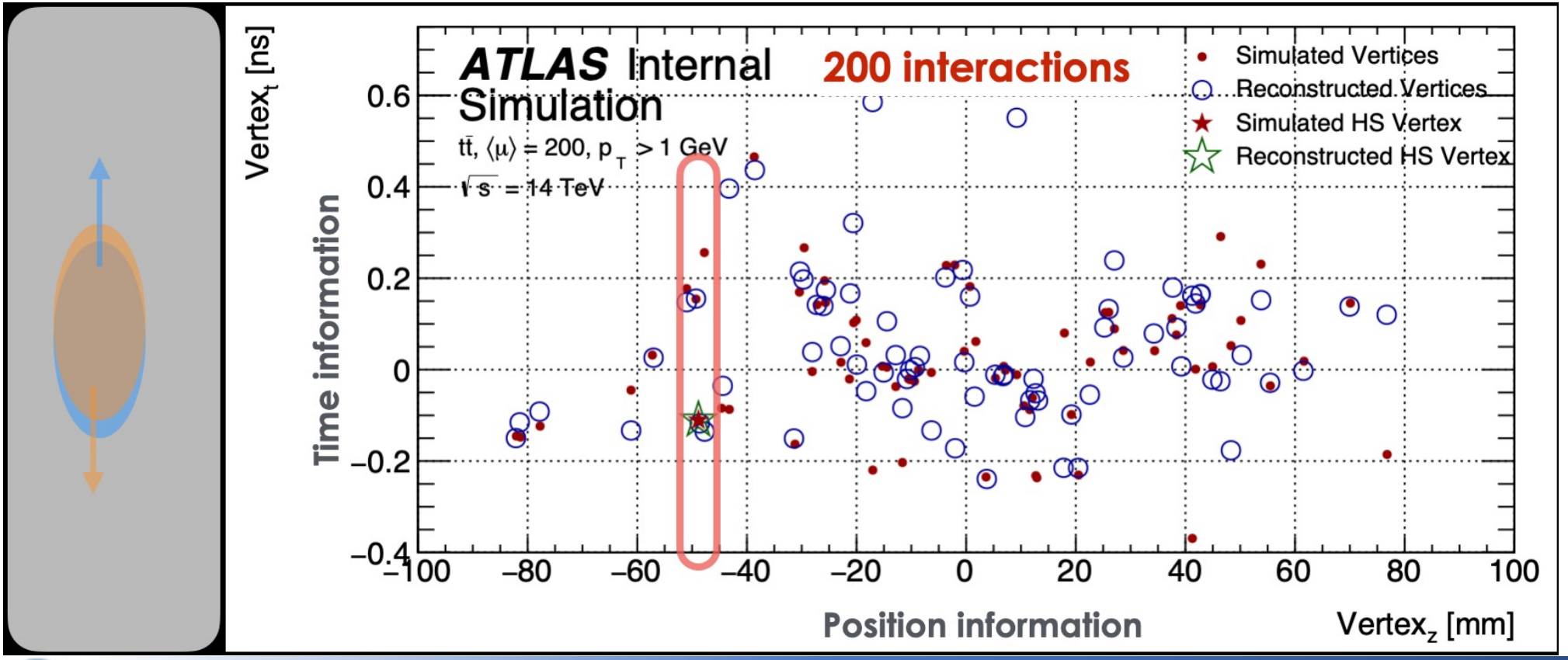
- High Luminosity LHC upgrade will happen in ~5 years
- One order of magnitude increase in instant luminosity compared to now



Current detectors cannot cope with such large rates, need:
Larger granularity
Faster trigger rates
New technologies (fast timing)

Motivation

- Pileup background is major challenges at high luminosity LHC
- High precision timing info can reduce the pileup by one order of magnitude



Motivation

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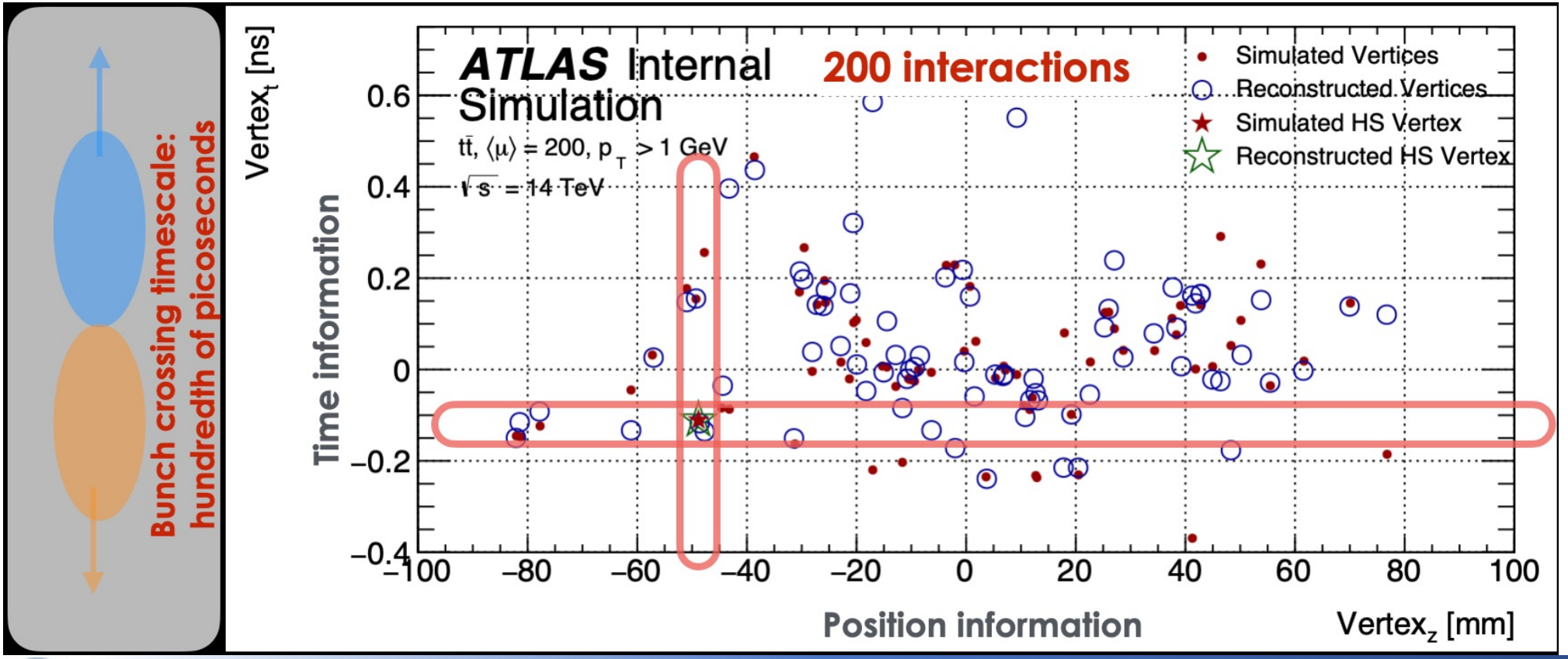
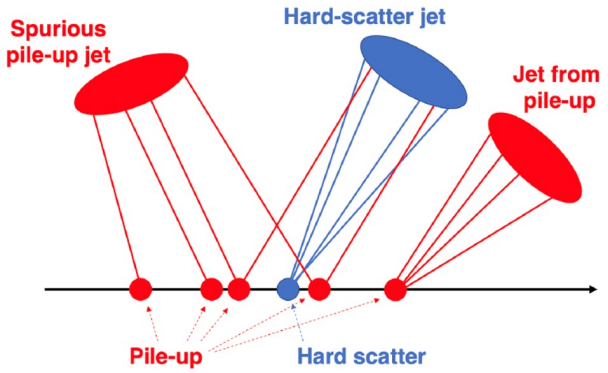
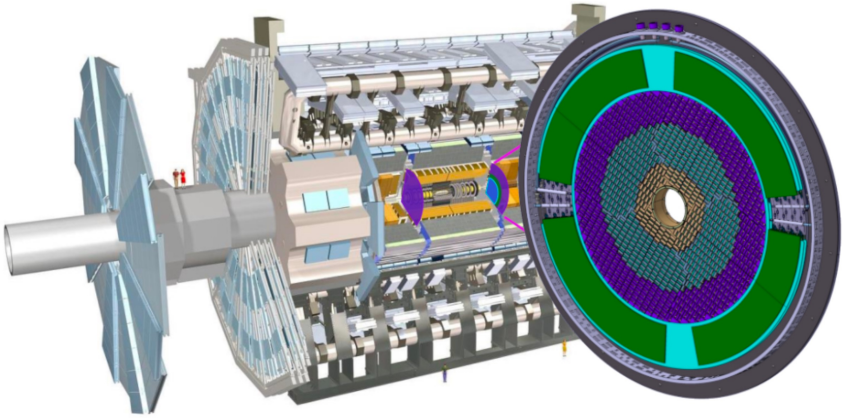


High Granularity Timing Detector (HGTD)

- **HGTD aim to reduce pileup contribution at HL-LHC**
  - **Timing resolution is required to be better than 30 ps (start) - 50 ps (end) ps per track**
- **6.4 m^2 area silicon detector and ~ 3.6 × 10^6 channels**
- **High Granularity: Pixel pad size: 1.3 mm × 1.3 mm**
- **Radiation hardness : 2.5x10^{15} N_{eq} /cm^2 and 2 Mgy**

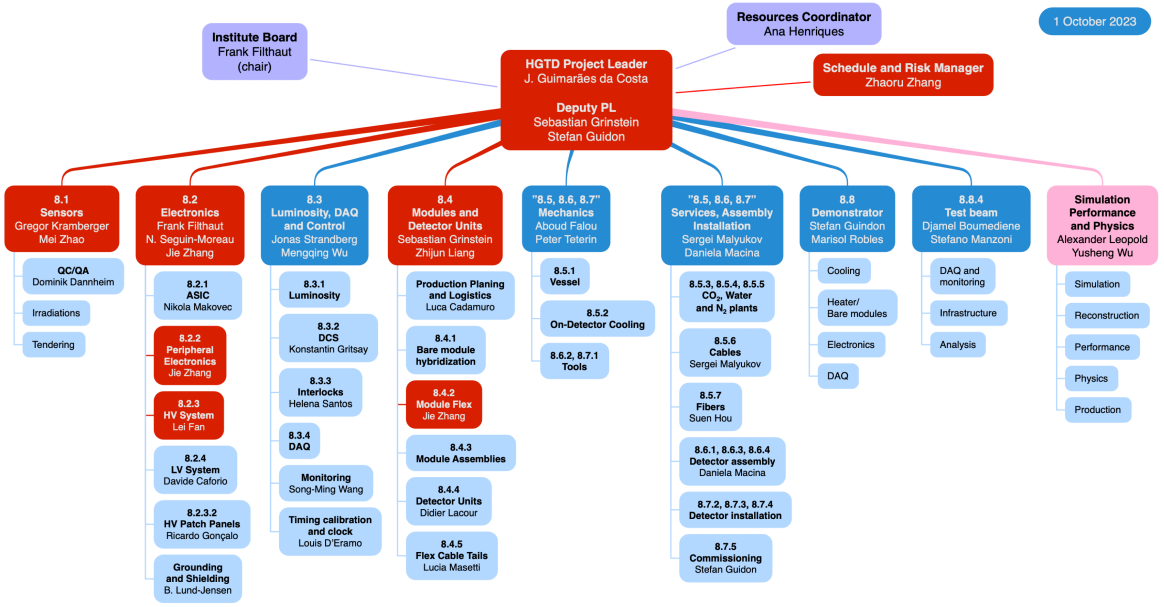


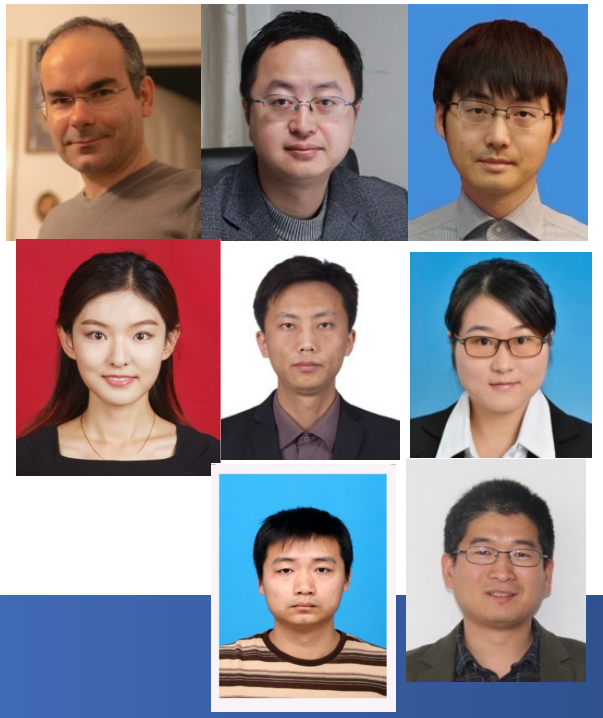
- **China team is making key contributions to HGTD**
  - **100% LGAD sensor (90% IHEP + 10% USTC)**
  - **44% detector assembly (34% IHEP + 10% USTC)**
  - **100% front-end electronics board (IHEP +NJU)**
  - **~33% flex tail (SDU)**
  - **50% ASIC testing (IHEP)**
  - **>16% high-voltage electronic systems (IHEP+ SDU)**
  - **Software and performance (USTC, IHEP)**



ATLAS China team in HGTD management

- ATLAS China team played a leading role in HGTD
  - Joao (IHEP) is re-elected as Project leader (2021-2025)，L1 manager
    - The first project leader in ATLAS China team
  - 5 Level-2 conveners (Module, Sensor, Electronics, Risk, Simulation)
  - 3 Level-3 conveners (PEB, high-voltage, module flex)
  - 1 Speaker committee



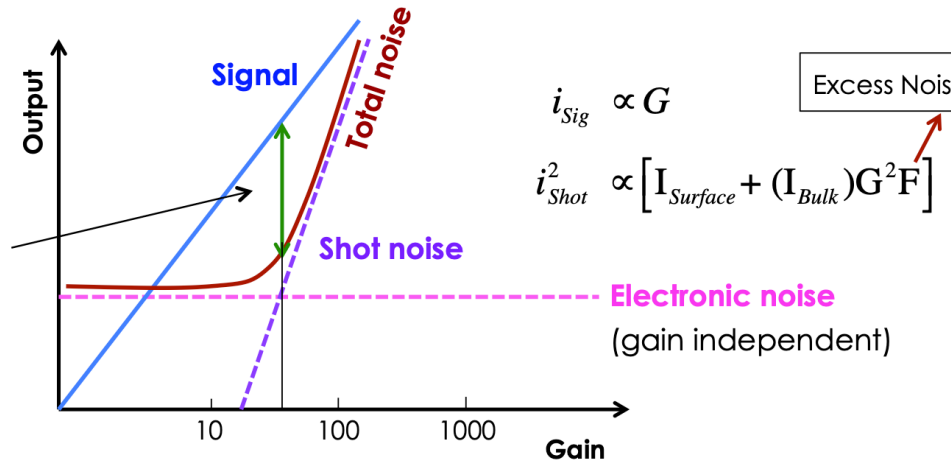


Low Gain Avalanche Detectors (LGAD)

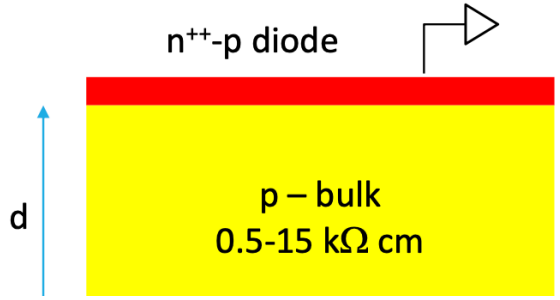
- Compared to APD and SiPM, LGAD has modest gain (10-50)
- High drift velocity, thin active layer (fast timing)
- High S/B, no self-triggering

$$\sigma^2_{jitter} = \left(\frac{t_{rise}}{S/N}\right)^2$$

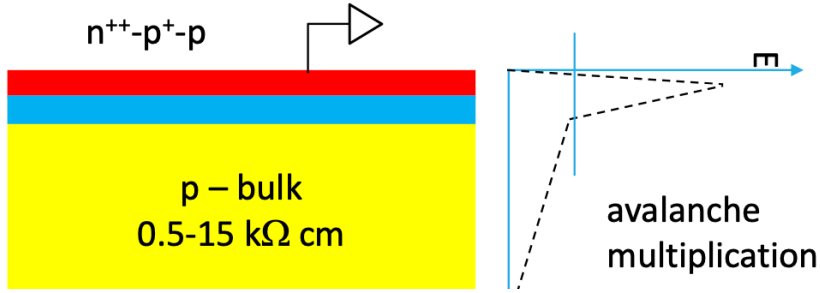
- **Modest gain to increase S/N**
- **Thin detector to reduce t_{rise}**



Conventional PiN diode

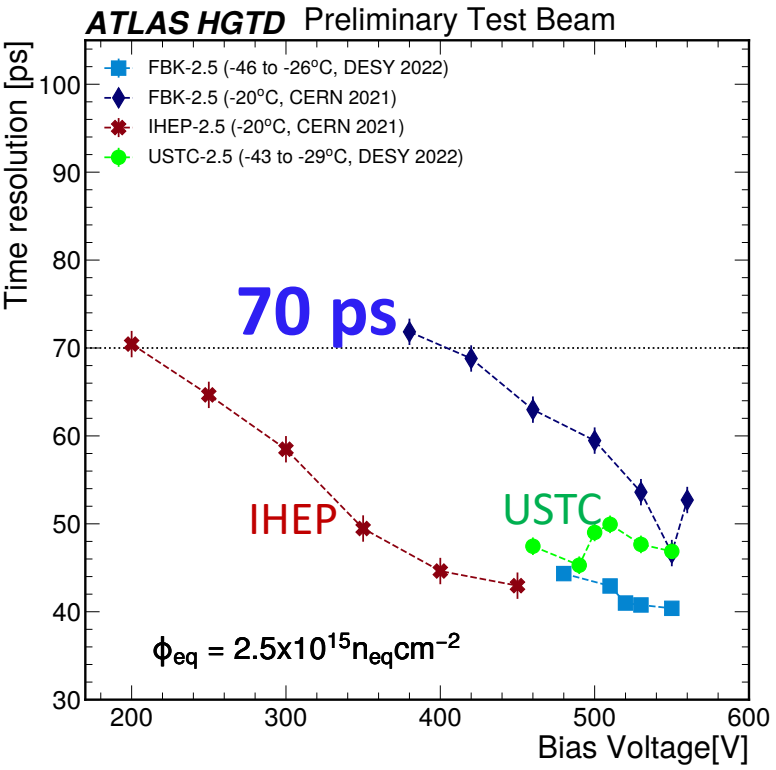


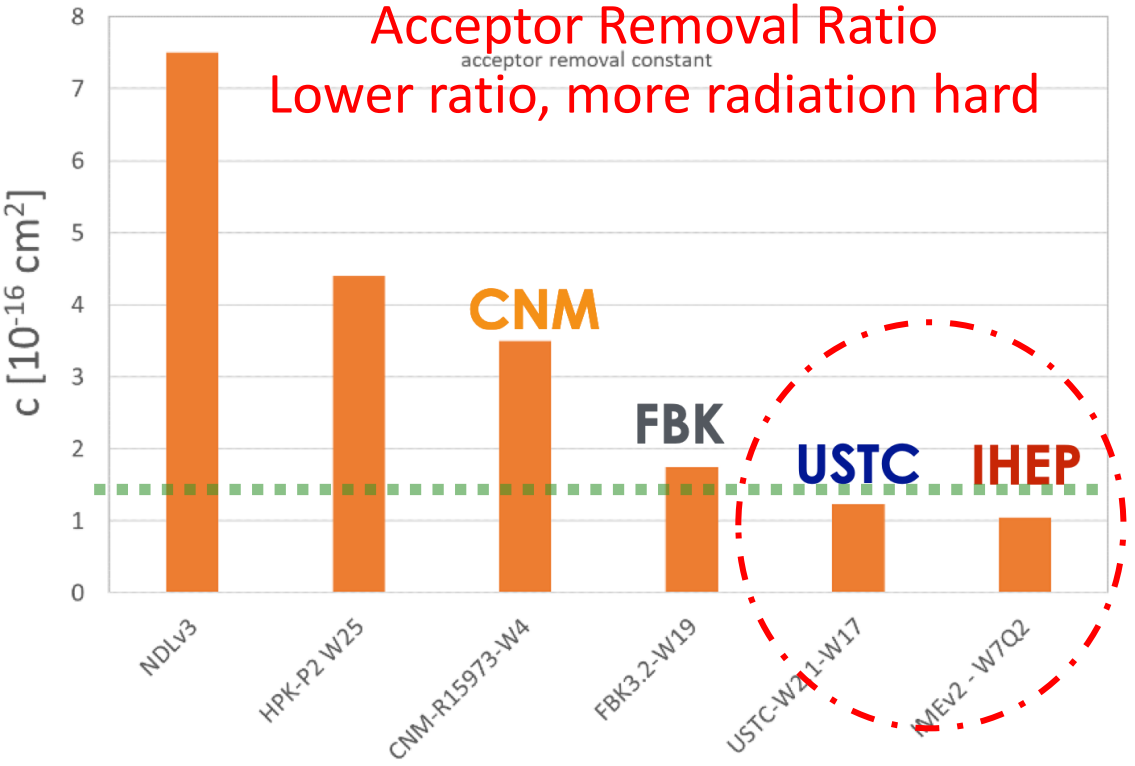
LGAD
P+ gain layer on top of PIN diode



LGAD sensor after Irradiation

- Lots of prototypes R&D in LGAD in last few years, active vendors includes:
  - IHEP-IME (China), USTC-IME (China), IHEP-NDL(China), FBK (Italy), CNM (Spain), HPK (Japan) …
- IHEP-IME and USTC-IME LGAD with carbon-enriched doping
  - Significantly lower acceptor removal ratio, the most radiation hard
- After 2.5×10^{15} n_{eq}/cm^2, LGADs can operated below 550 V → avoid single event breakdown



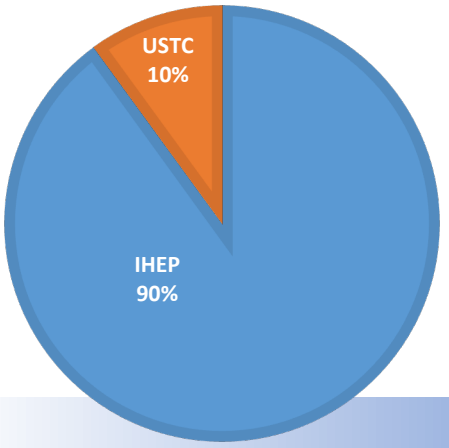


LGAD sensors pre-production

More details in Mei Zhao's talk

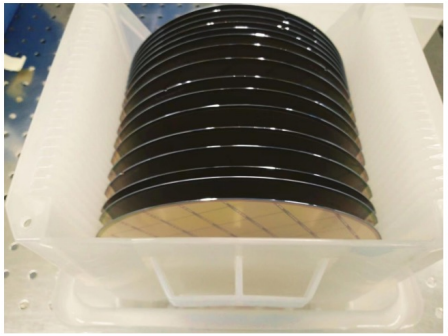
- In May 2013, CERN chosen IHEP-IME in HGTD sensor tendering.
  - First time domestic silicon sensor was chosen by CERN in LHC experiment
  - Won the competition with Hamamatsu (Japan) and FBK (Italy)
- The current production plan:
  - IHEP-IME: 90% (66% from CERN tendering+24% in-kind contribution)
  - USTC-IME: 10% in-kind contribution

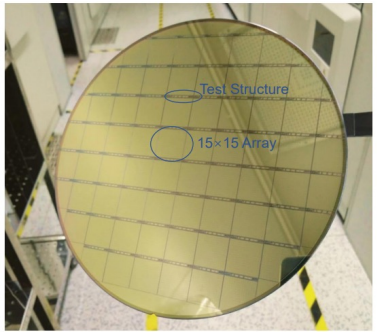
Share of production
Share between vendors



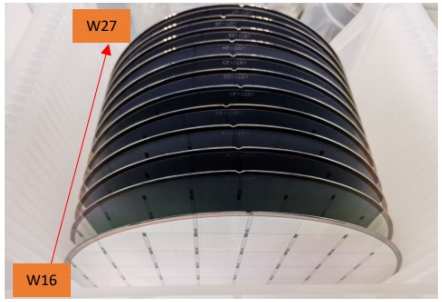
Pre-production LGAD sensors from China

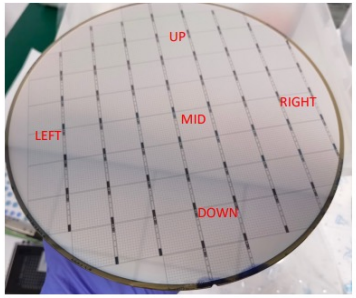
IHEP-IME
Pre-production





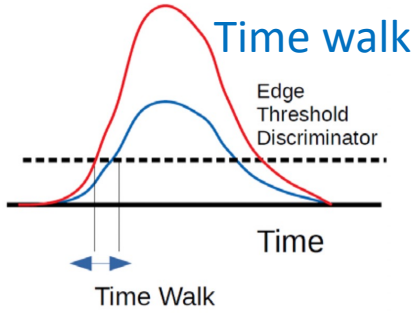
USTC-IME
Pre-production



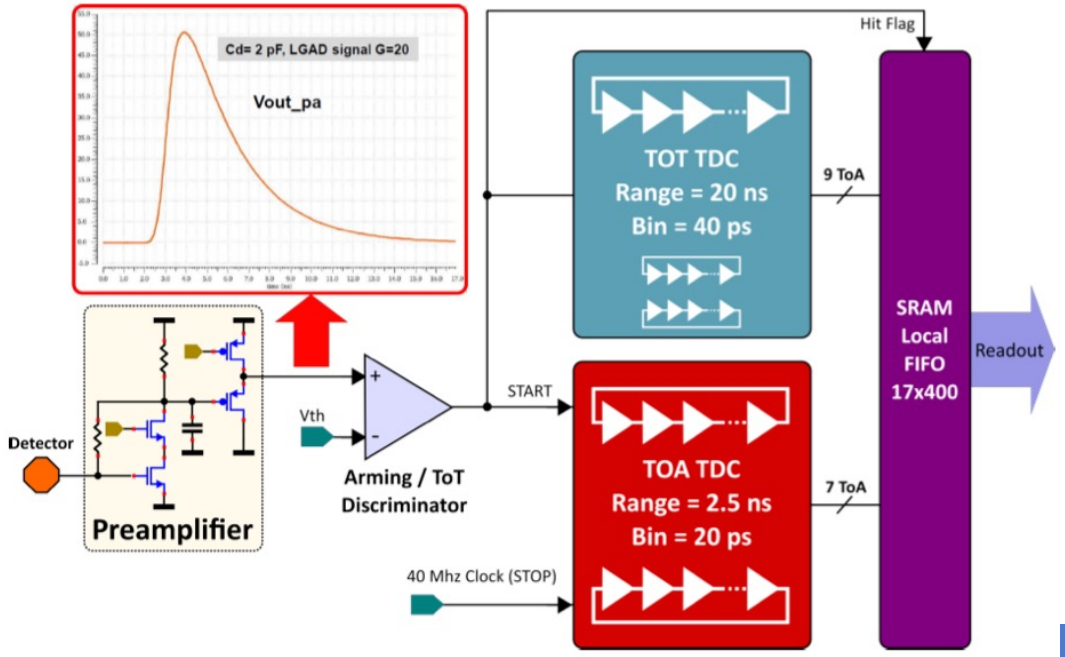


ALTIROC : Fast Timing ASIC

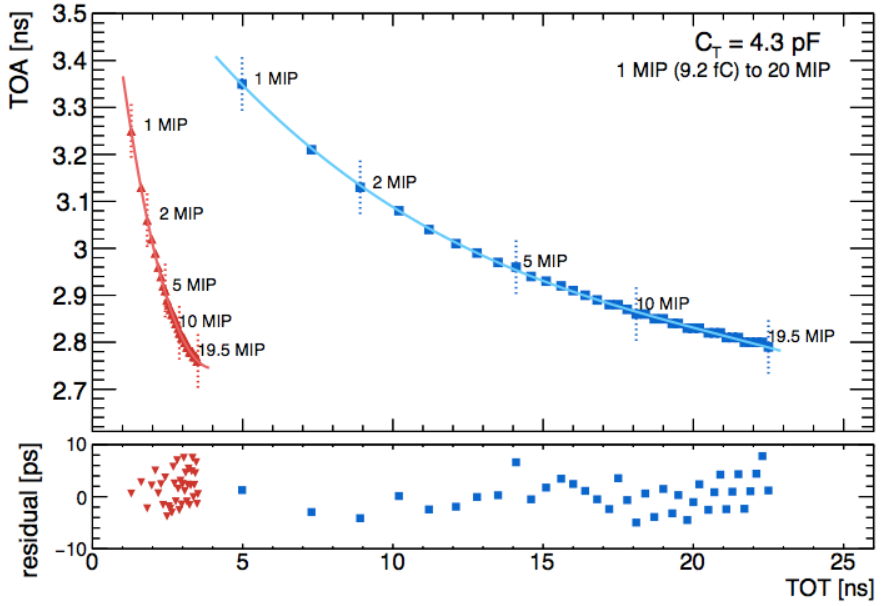
- 225 front-end channels in ALTIROC, each channel has
  - A preamplifier followed by a discriminator:
  - Two TDC (Time to Digital Converter) to provide digital **Hit data**
    - Time of Arrival (TOA) : Range of 2.5 ns and a bin of 20 ps (7 bits)
    - Time Over Threshold (TOT) : range of 20 ns and a bin of 40 ps (9 bits)
  - One Local memory: to store the 17 bits of the time measurement until L0/L1



ALTIROC timing ASIC in nutshell



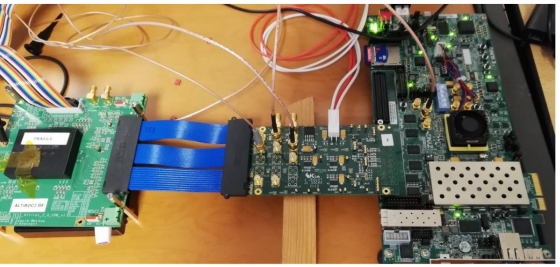
Time walk correction with TOT



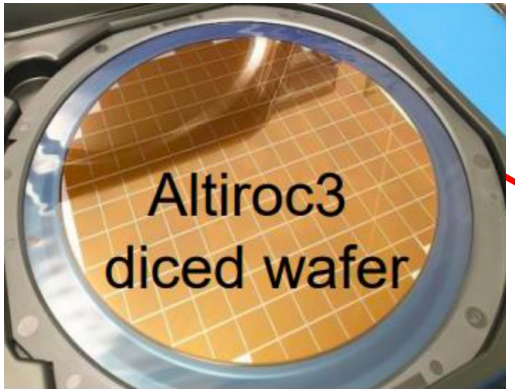
ALTIROC R & D

- IHEP is responsible for 50% of ALTIROC ASIC wafer testing
  - IHEP joined the digital part of ALTIROC ASIC design
- ALTIROC2/ ALTIROC3– 15x15 array with almost complete functionalities
  - ~15 ps jitter @ 15 fC, better than 70 ps jitter@ 4 fC
  - Full-size ASIC prototype ~2x2 cm^2 with 225 readout channels
  - Large amount of digital data, limited power consumption (1.2W/ASIC → 5.3 mW/ channel)

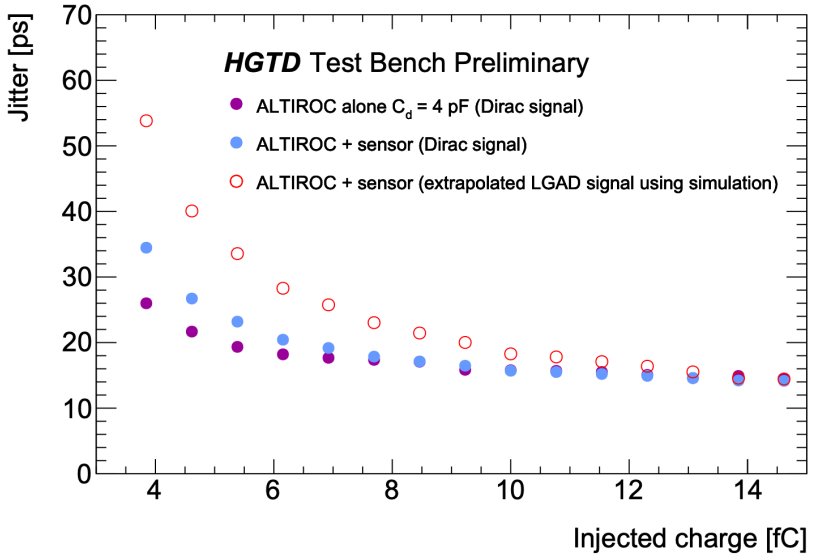
ALTIROC and test boad



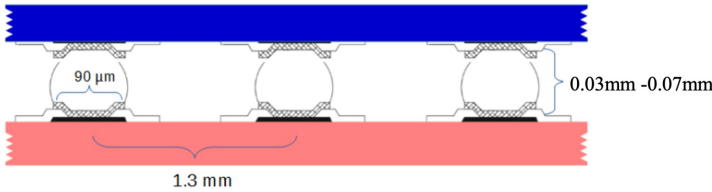
ALTIROC3 wafer@IHEP



Injected charge Vs jitter



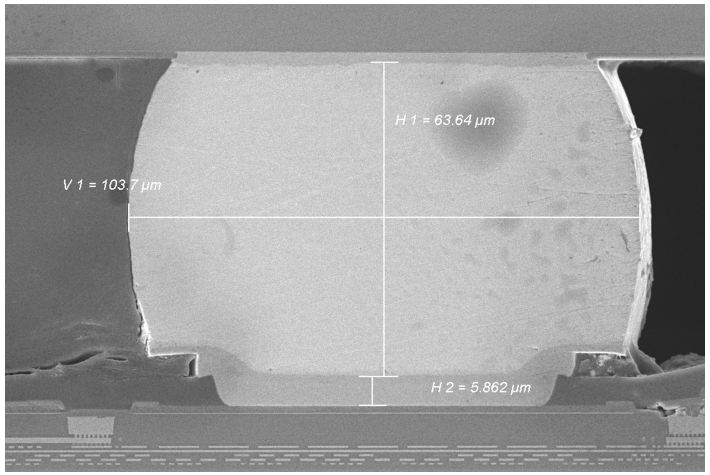
ALTIROC3 full-size hybrid



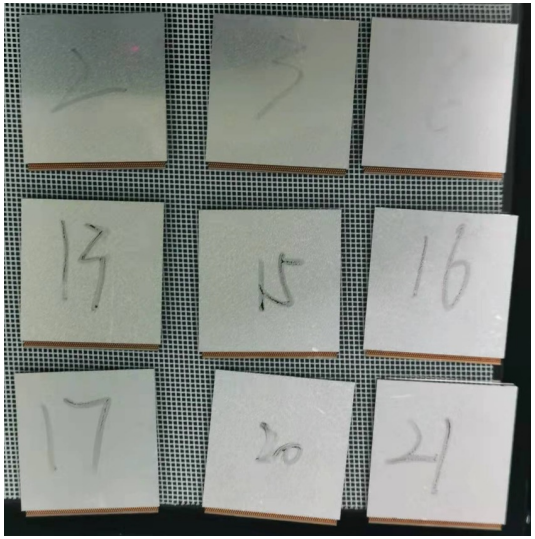
- Full Size ALTIROC3 full-size bare by different institutes and companies
  - IHEP is contributing 50% of hybrids
  - IHEP made prototype with ALTIROC2 ASIC + IHEP-IME LGAD sensor

More details in Xuan's talk

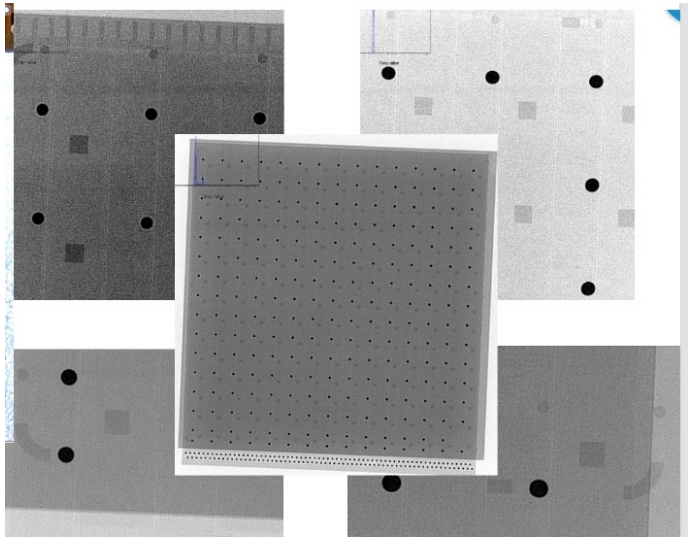
Bump connection in hybrid profile view



ALTIROC ASIC + IHEP-IME LGAD

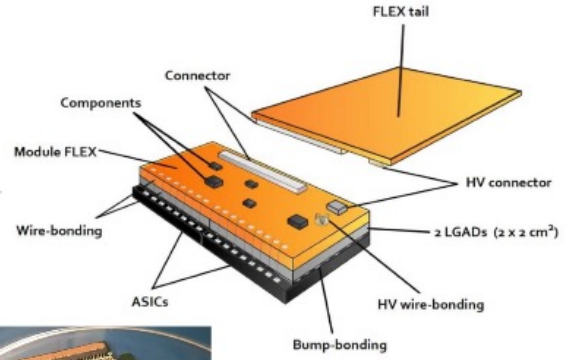


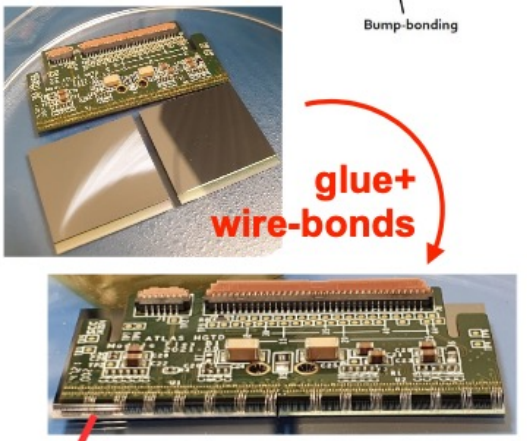
X-ray image of full-size hybrid

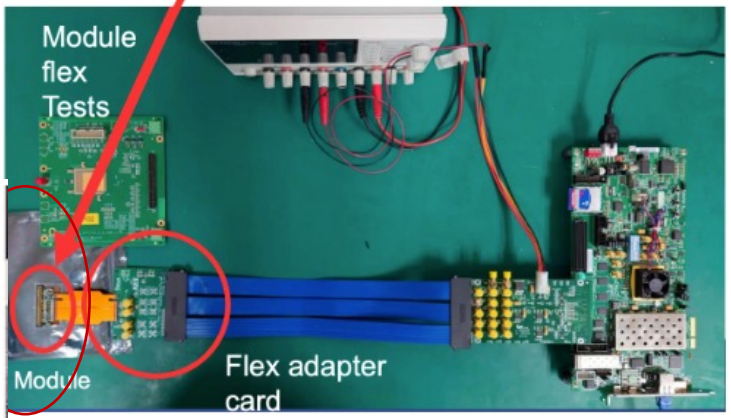


HGTD module assembly

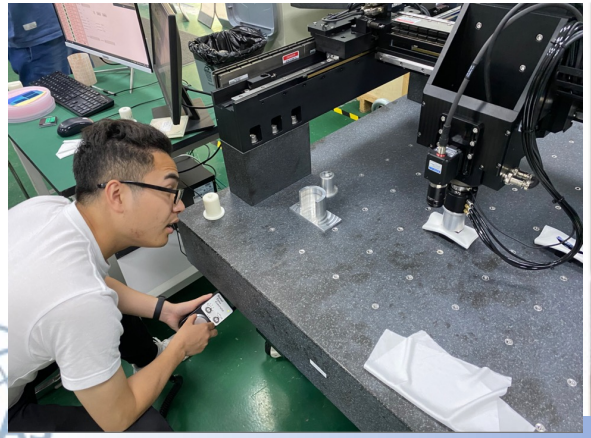
- China is responsible for 44% of module
- 6 module assembly site at HGTD
  - IHEP, USTC, Mainz, France, IFAE, Morocco
  - IHEP is largest site, 34% module assembly (~3000)
  - USTC is responsible for 10% of assembly
- IHEP developed gantry system
  - Automatic glue dispending
  - Pattern recognition, automatic assembly



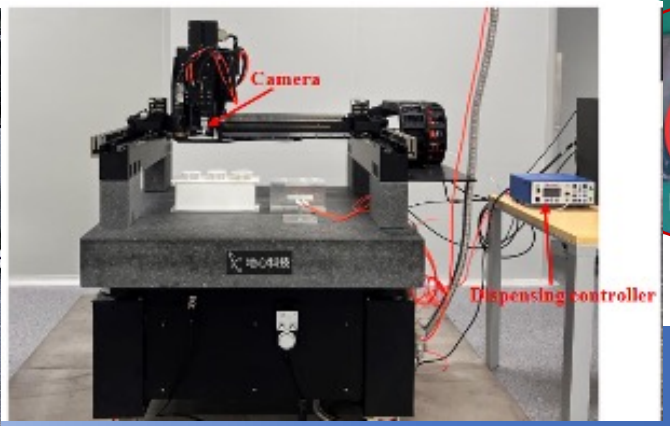




Gantry @ IHEP



Gantry @ USTC

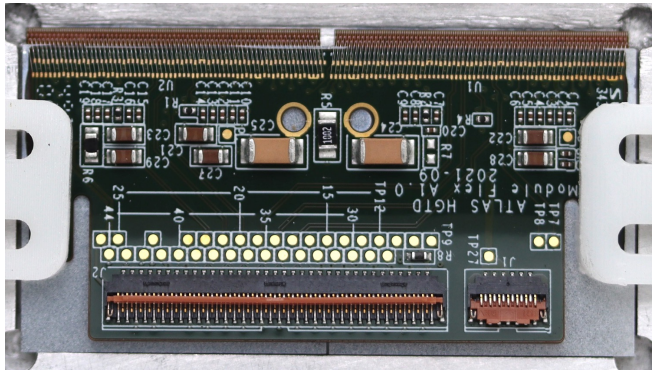


HGTD Module assembly

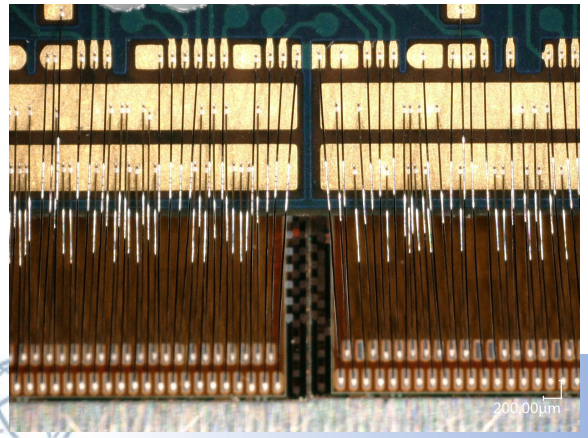
- IHEP made the first of ALTIROC2 and ALTIROC3 modules in HGTD

More details in Xuan's talk

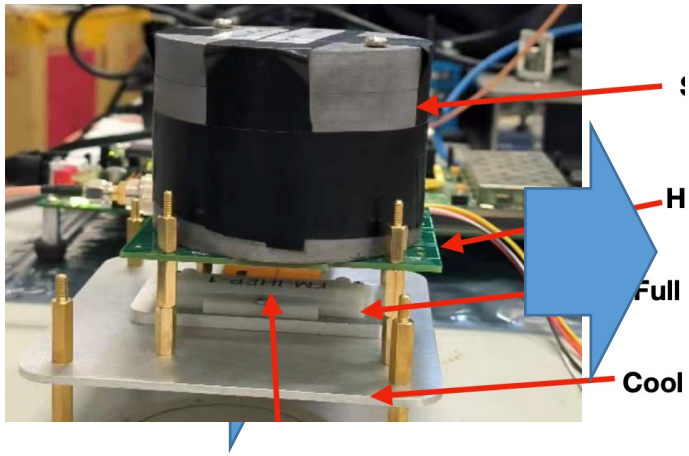
IHEP ALTIROC2 module



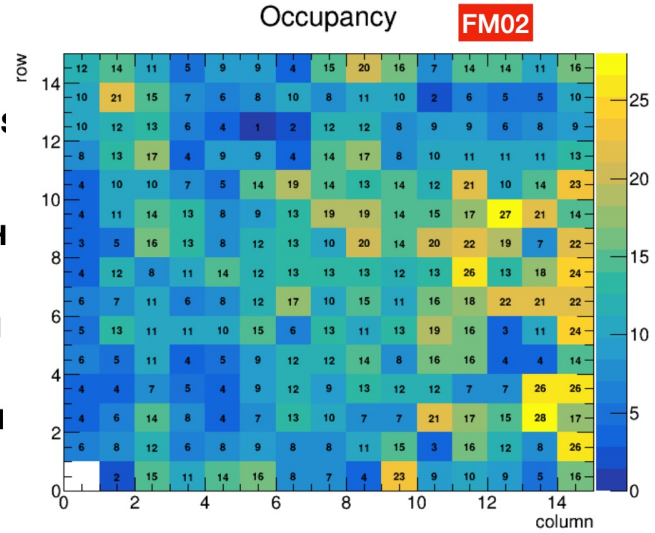
IHEP ALTIROC3 module



Beta source test setup

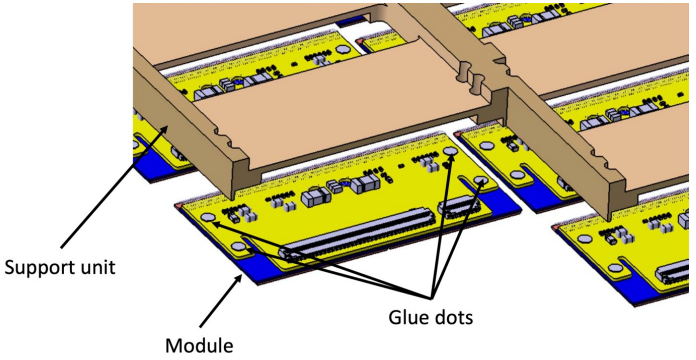


Hit maps in beta source test



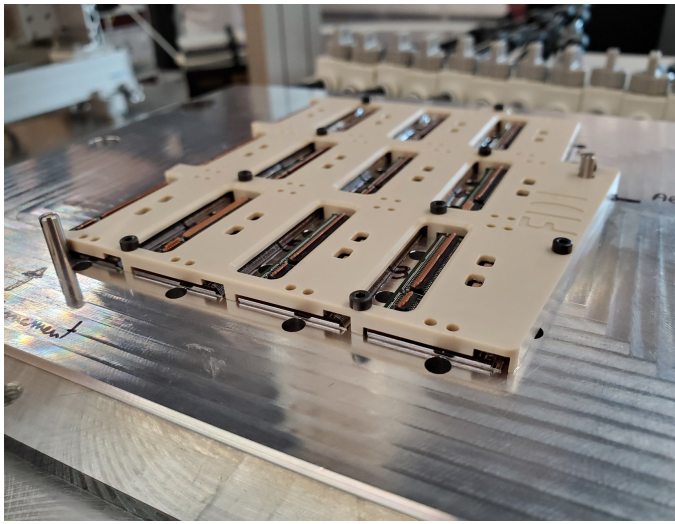
HGTD detector unit

- IHEP is responsible for 50% of support unit
- Modules are installed and glued on support units
  - Challenges :machining of PEEK (flatness <200μm)

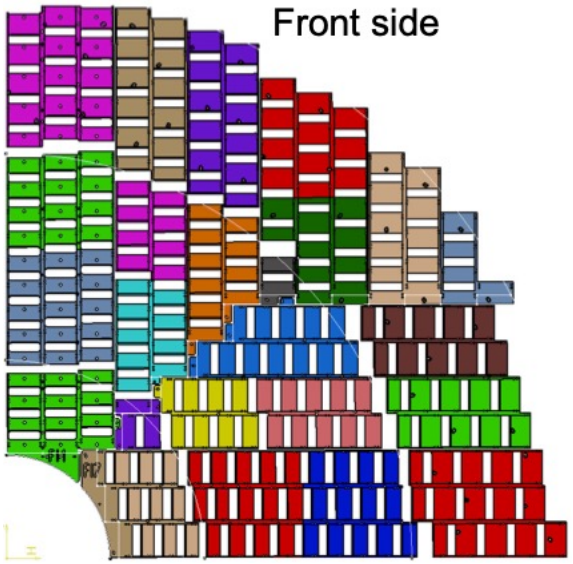


More details in Xinhui's talk

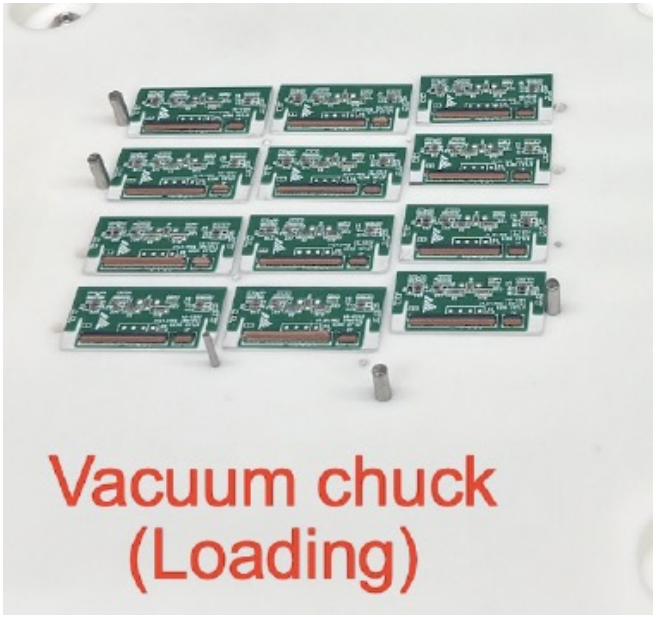
Loading modules on support units



Different color represents different support units.



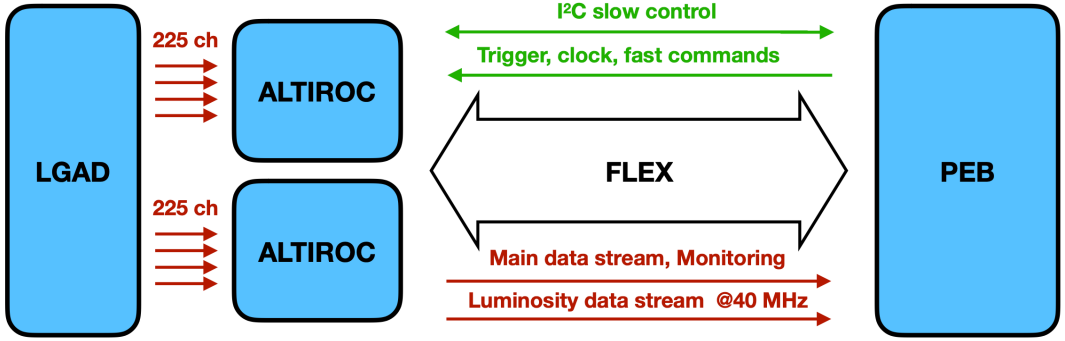
Gluing modules on support units



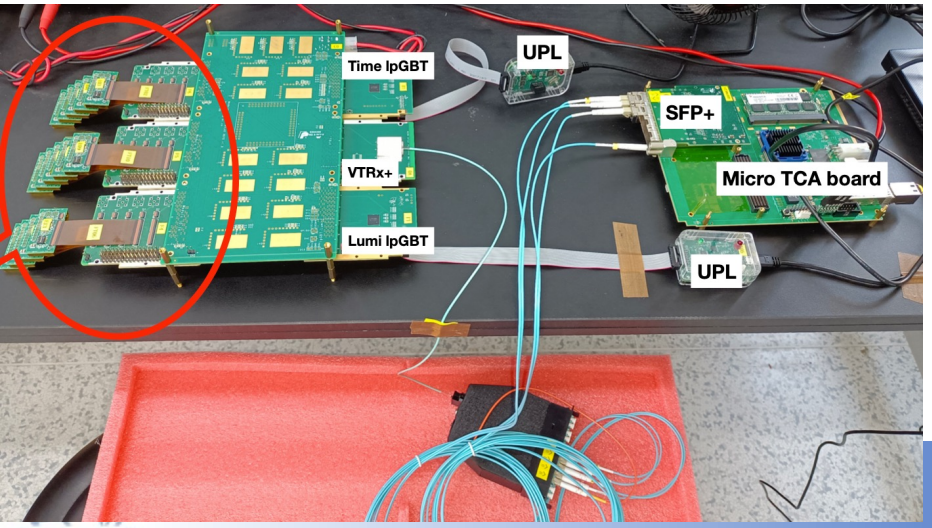
Peripheral Electronics Boards, flex tail, HV power supply

- IHEP and NJU developed Peripheral Electronics Boards prototype
- SDU developed long flex tail prototype (75cm)
- IHEP developed high voltage power supply prototype

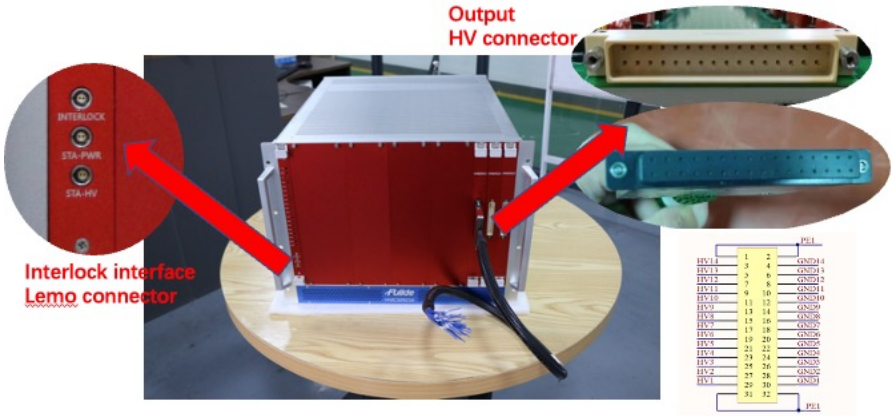
More in ZhenWu
Mingjie, Chuanyi's talk



Modular Peripheral Electronics Boards prototype



High voltage power supply prototype



Long Flex tail prototype (75cm)

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Summary

- China team is playing leading role in HGTD detector
  - Joao (IHEP) is re-elected as Project leader (2021-2025)
  - Many Level-2 and Level-3 convenorship
- China team will provide 100% of LGAD sensor (90% IHEP, 10% USTC)
  - CERN chosen IHEP-IME LGAD sensor in HGTD sensor tendering
- ALTIROC 3 (full size ASIC) on schedule, so far all blocks functional
- Module assembly is in progress
  - IHEP produced the first batches modules with ALTIROC2 and ALTIROC3
- Prototyping of some Peripheral Electronics Boards, flex tails and HV supply
- Next milestones:
  - 2023: Peripheral electronics boards and LGAD sensors production started
  - 2024: ASICs, Modules and detector units production started
  - 2026-2027: HGTD detector Integration at CERN, installation