The Prototype Design of PEB

a Component of the HGTD On-detector Electronics for the ATLAS Phase-II Upgrade

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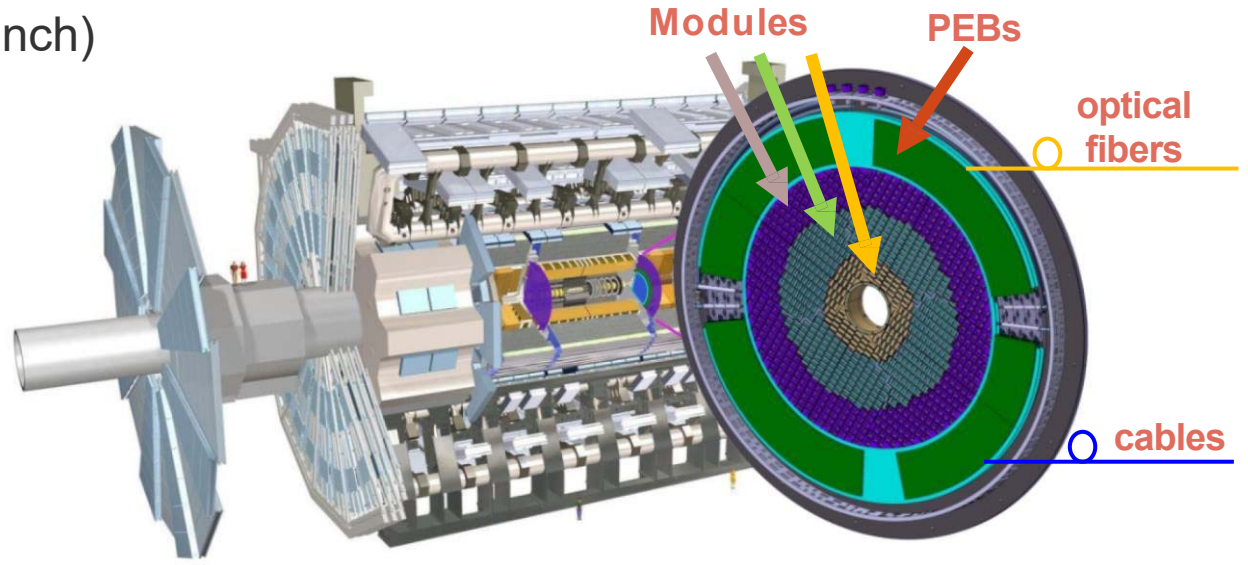
Introduction

❑ High Granularity Timing Detector (HGTD)

- ➢ Silicon detector with coarse spatial resolution but precise timing
- ➢ ~3.6 million 1.3×1.3 mm2 pixels with Low-Gain Avalanche Detector (LGAD) technology
- ➢ 6.4 m^2 active area
- ➢ Pileup rejection
  - Time resolution at the start (end): 30 (50) ps per track / 35 (70) ps per hit
- ➢ Luminosity measurement
  - Count number of hits at 40 MHz (bunch-by-bunch)
  - Goal for HL-LHC: 1% luminosity uncertainty
- ➢ Detector structure
  - Two end-caps
  - $z \approx \pm 3.5$ m from the nominal interaction point
  - $110 < r < 1000$ mm
  - Active detector region: $2.4 < |\eta| < 4.0$



Global view of the HGTD

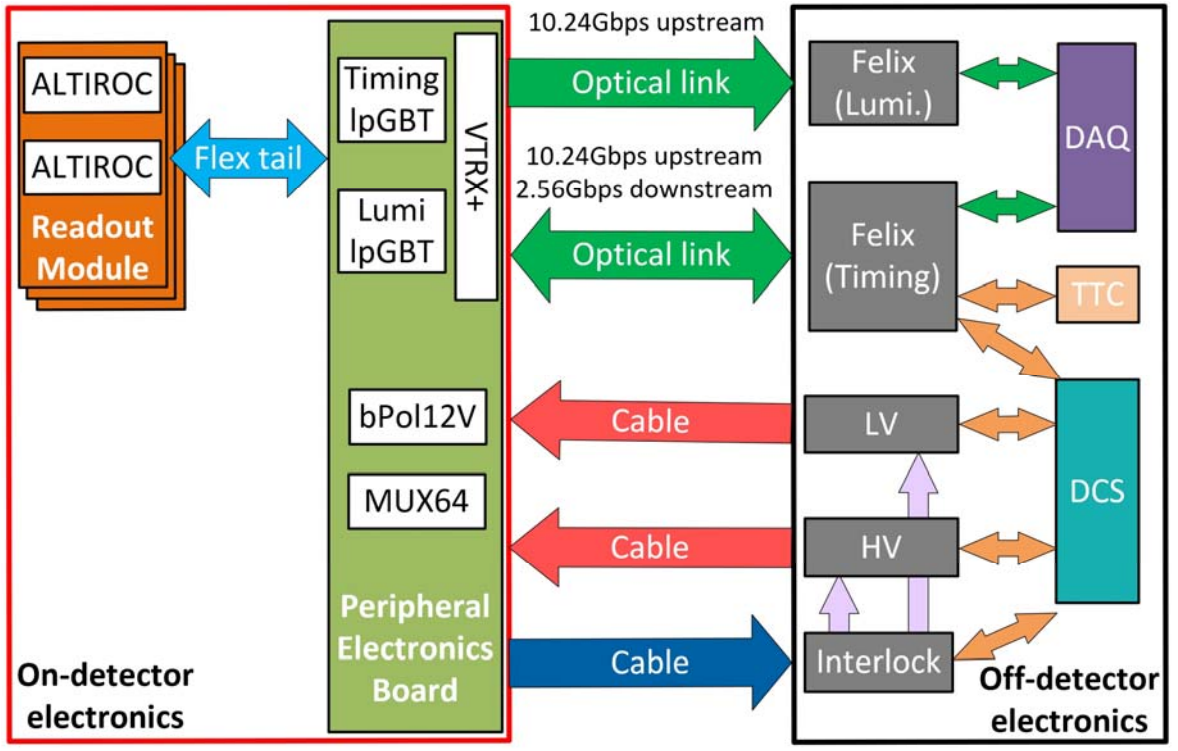
Overview of HGTD Readout Electronics

❑ On detector

- ➢ Front-end modules
- ➢ Flex tail cables
- ➢ Peripheral Electronics Boards
  - Contains 4 types of chips: bPol12V, MUX64, lpGBT and VTRX+ (***REF. CLHCP2022***)

❑ Off-detector

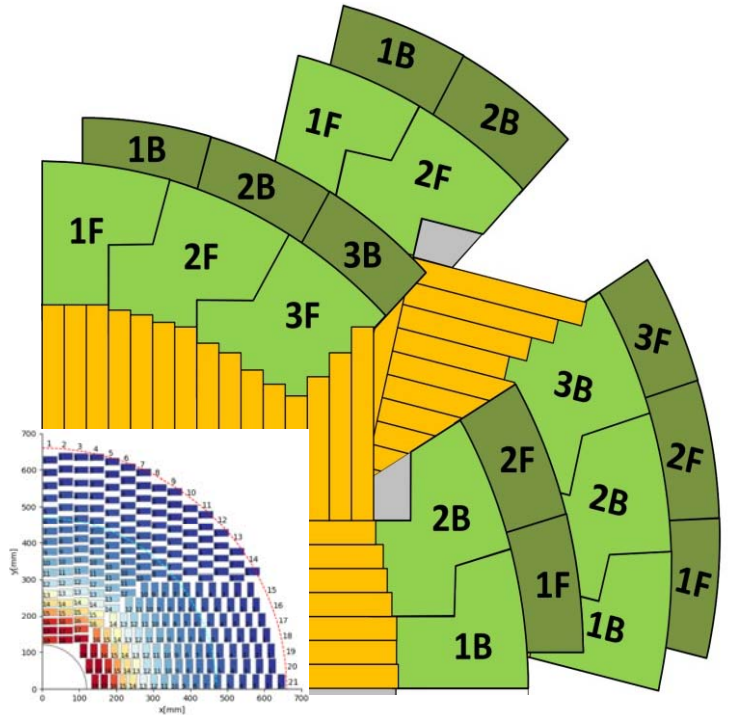
- ➢ Data Acquisition System (DAQ)
- ➢ Luminosity System
- ➢ Timing, Trigger and Control (TTC)
- ➢ Detector Control System (DCS)
- ➢ Low Voltage (LV)/High Voltage (HV) system
- ➢ Interlock system



HGTD electronics architecture

Peripheral Electronics Boards(PEB)

- Six types of PEB (front and back side)
- Board 1F, 2F, 1B and 2B are used on both sides
- Each board connects a similar number of modules
- The front-end modules are connected via flex tails, arranged in rows, to the PEB @ 660 < r < 920 mm
- 80 boards per end-cap, thus 160 boards in total
- Basic functions of PEB
  - Control, monitoring & data aggregation and transmission
  - Power-supply distribution: LV & HV
  - Thermistor connection between the front-end modules and the interlock system
- Design and production
  - Designed by IHEP, NJU and Morocco group. Produced by IHEP (50%) and NJU(50%)

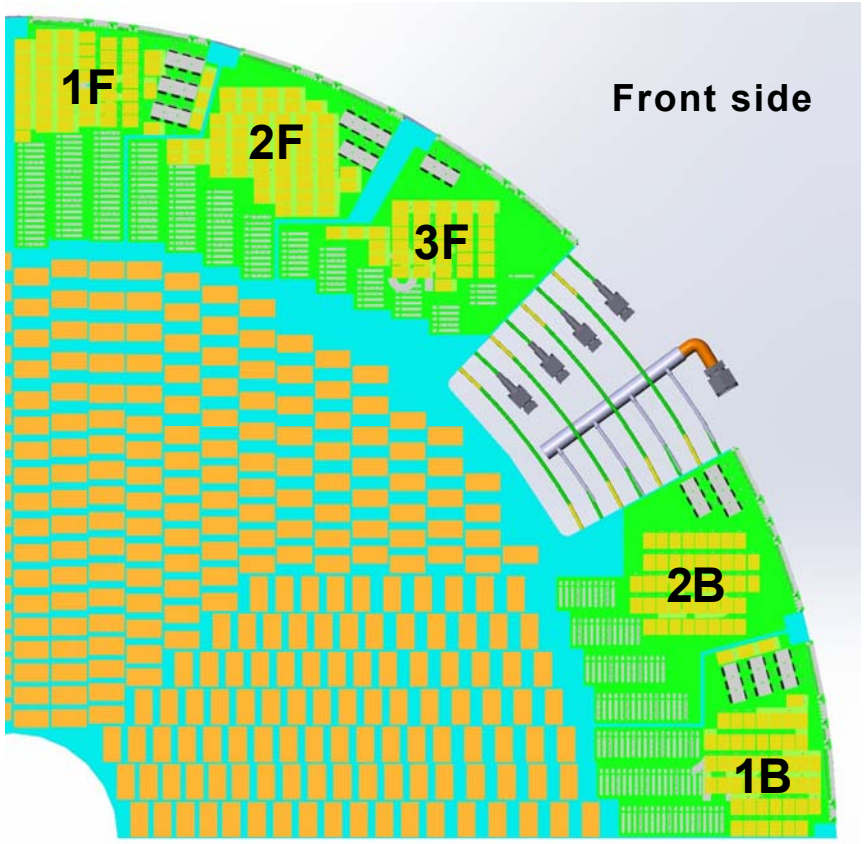


One quadrant of the two instrumented disks

PEB	Front side	Back side	Quantity
1F	54 modules	55 modules	32
2F	52 modules	56 modules	32
3F	39 modules	-	16
3B	-	39 modules	16
2B	52 modules	48 modules	32
1B	54 modules	53 modules	32

Requirements in PEB Design

- ❑ Area and height restrictions
  - ➢ Limited surface area for thousand of components and nets
  - ➢ Height < 10 mm
- ❑ Connecting 8032 front-end modules
  - ➢ Up to 50k analog monitoring
  - ➢ Up to 10 Tbps to TDAQ, on average, 63 Gbps per PEB
- ❑ LV & HV power-supply distribution
  - ➢ Low noise, heat dissipation, system level shielding and grounding considerations
- ❑ Thermistor connection between the front-end modules and the interlock system
  - ➢ 896 Negative Temperature Coefficient (NTC) sensors to monitor disk temperature



One quadrant of the two instrumented disks

Requirements in PEB Design

❑ Radiation tolerance for PEB

	From simulation	Safety factor	Design requirement
Si 1 MeV neutron equivalent	< 1.4 x 10^{15} neq /cm^2	1.5 x 1.3	2.73 x 10^{15} neq /cm^2
Fluence of hadrons > 20 MeV	< 0.32 x 10^{15} neq /cm^2	1.5 x 1.3 x 2	1.25 x 10^{15} neq /cm^2
TID	< 36 Mrad (0.36 MGy)	1.5	54 Mrad (0.54 MGy)

❑ Magnetic field

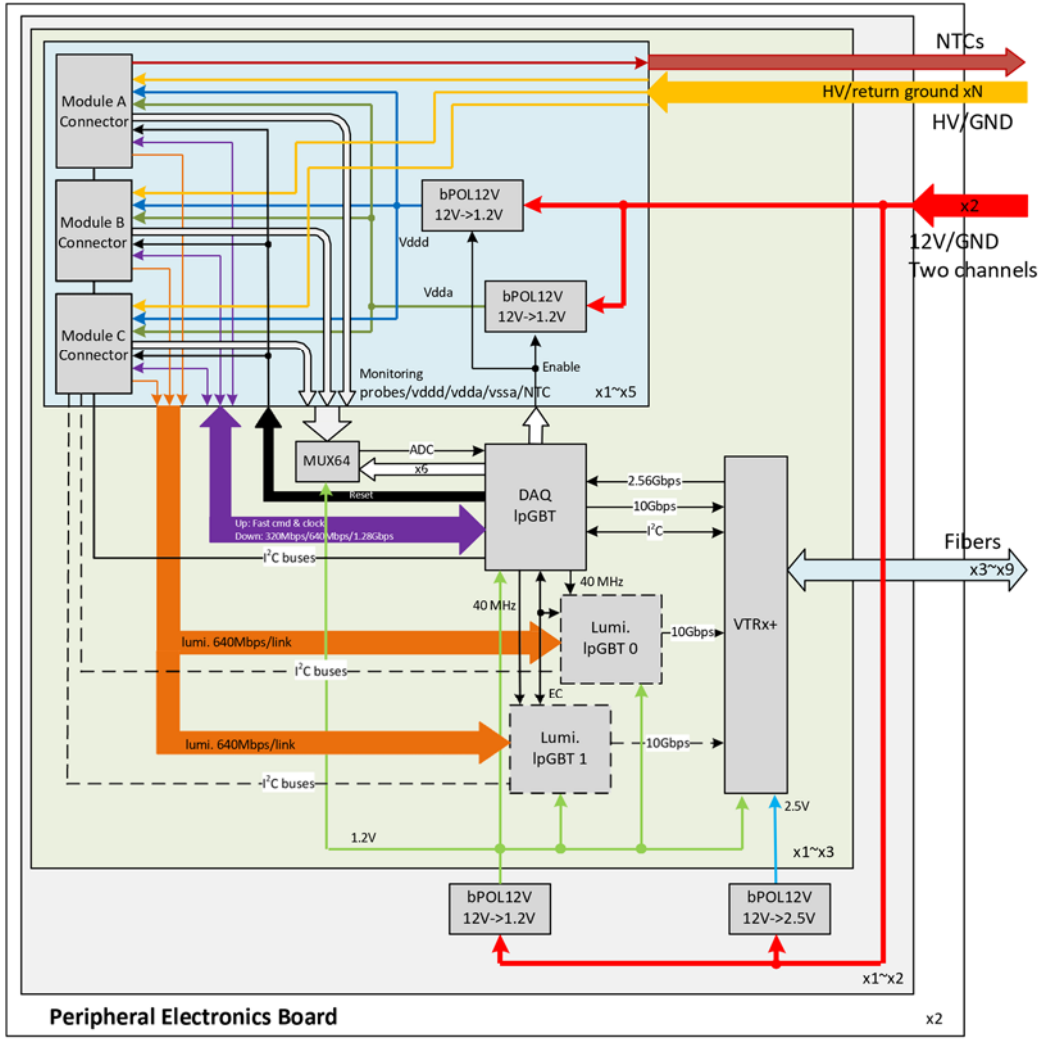
- Amplitude: 0.382 T ~ 0.433 T
- Angle 23.1° ~ 32.3°

❑ Operating Temperature:

- On disk (with front-end modules and CO2 cooling): -35 ℃ ± 5 ℃
- Testing/debugging (with cooling): -40 ℃ to 55 ℃

Conceptual Design of PEB

- Two LV channels to dozens of bPol12V chips
  - Provide 1.2V for the ALTIROCs
    - Up to 3 modules share two bPOL12v
    - One for analog power, the other for digital power
  - Provide 1.2V and 2.5V for the chips on PEB
- One timing lpGBT and 1~2 luminosity lpGBTs share one VTRx+
  - Bi-directional slow control and monitoring communication between the FELIX and the lpGBT
  - Timing/luminosity data to FELIX
- Control
  - I2C of lpGBT
    - Each lpGBT has 3 I2C master
    - Module and VTRx+ configuration



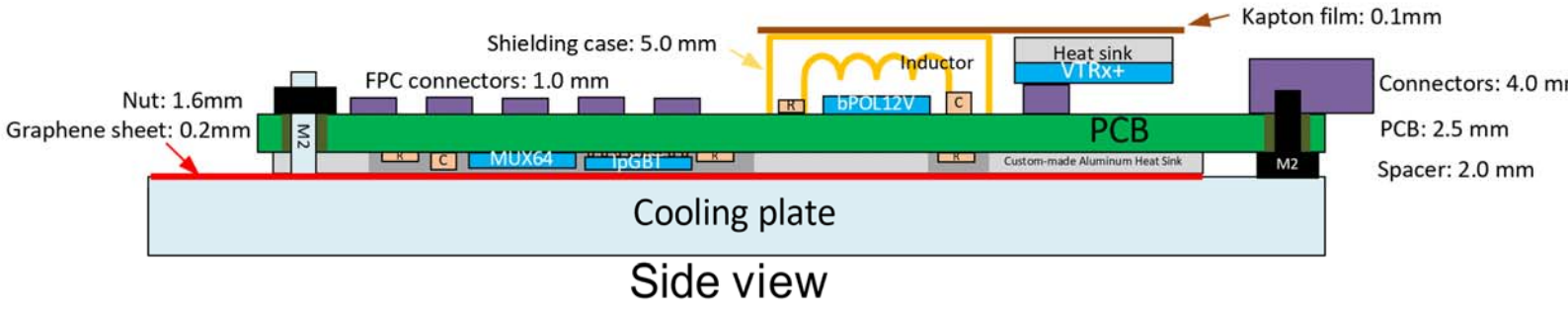
Conceptual Design of PEB

- ❑ Output to modules
  - ➢ Reset
  - ➢ Clock
  - ➢ Fast command
- ❑ Input form modules
  - ➢ Timing/luminosity data
- ❑ Monitoring
  - ➢ Each lpGBT has a 8 channel multiplexed ADC
  - ➢ Module state monitoring
    - VDDA, VDDD, GNDA, PROBE0/1(internal state and temperature), NTC
  - ➢ PEB state monitoring
    - lpGBT voltage, temperature
    - VTRx+ RSSI(average optical power of the received light) and NTC
    - bPOL12v temperature
    - bPOL12v power good signal
    - On board NTC
  - ➢ an external 64-to-1 MUX is required: MUX64

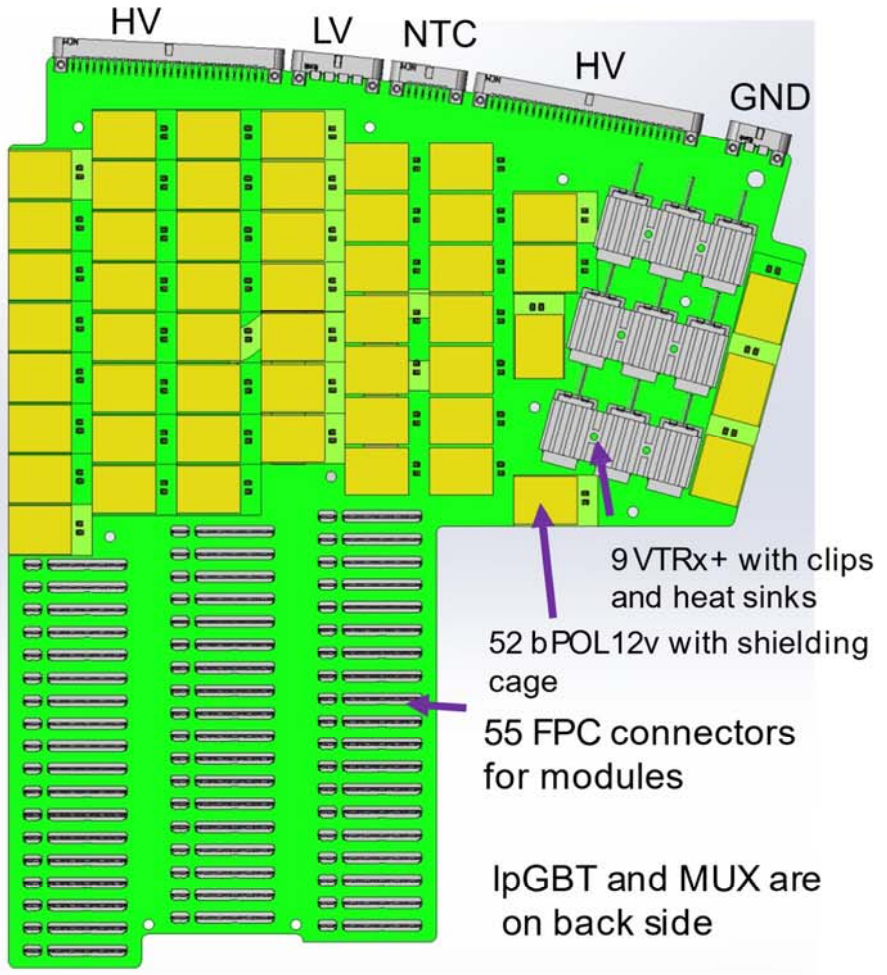
PEB 1F Design

PEB	Modules	lpGBT	MUX64	bPOL12v	VTRx+
1F	55	9+3	9	52	9

- Key dimensions
  - PCB thickness: 2.5 mm
  - 55 FPC connectors
    - Center to center distance: 6.5 mm
  - 52 bPOL12v power blocks
    - Size: 24 mm x 14.5 mm
    - Height above PCB: 5 mm
    - Height under PCB: 2 mm



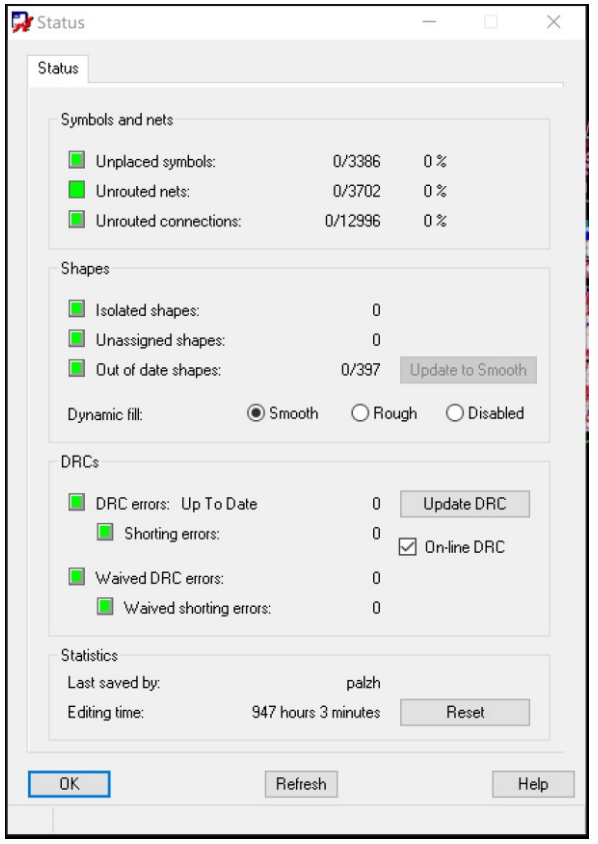
Side view

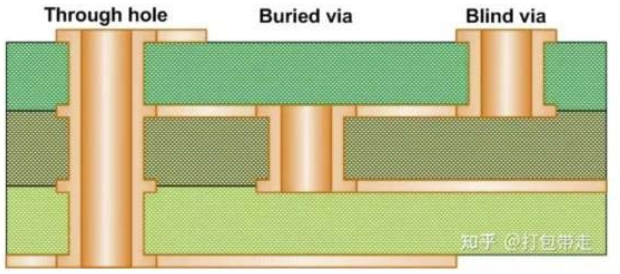


Top view of PEB 1F

PEB 1F Design

- Complex PCB
  - High speed, low loss material
    - Impedance control
  - Halogen free
    - EM-890 or IT-170/988 or R-5375(E)
  - Symbols and nets
    - 3386 components, 12996 connections
  - 22 layers PCB for PEB 1F, includes:
    - 8 layers for signals
    - 2 layer for HV and HV return ground
    - 4 layers for ground
    - 8 layers for power
  - HDI (High Density Interconnector)
    - Micro via



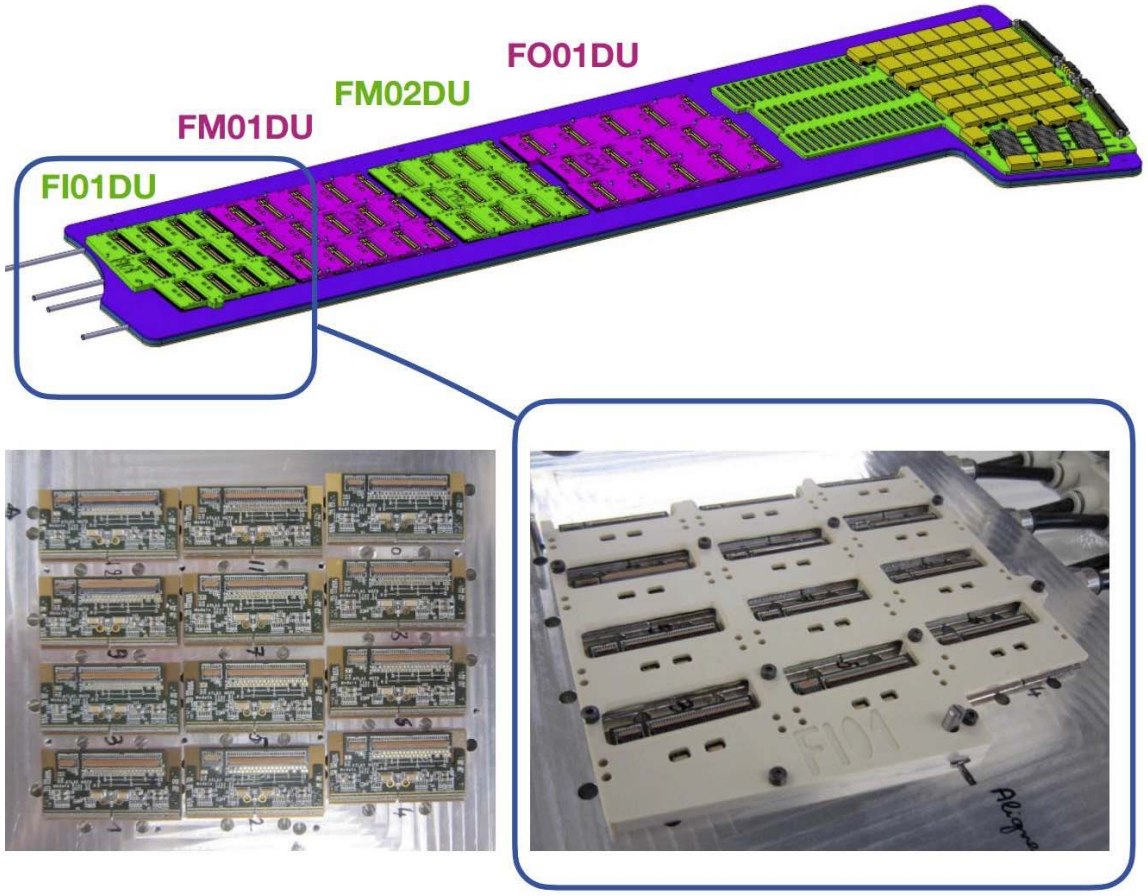


VIPPO / POFV: Via-in-Pad Plated Over PCB

Conclusion and Outlook

- PEB 1F prototype is under production
- HGTD on-detector electronics moving towards the FDR phase
- Focus on the full demonstrator
  - Electronics : 54 modules mounted on 4 support units + flex tails + PEB 1F + LV + HV

Many challenges ahead, but remarkable technical progress achieved



Thank you !