



Sensor test of CMS ETL of MTD in USTC

Chengjun Yu, Nan Lu

University of Science and Technology of China

On behalf of CMS MTD group

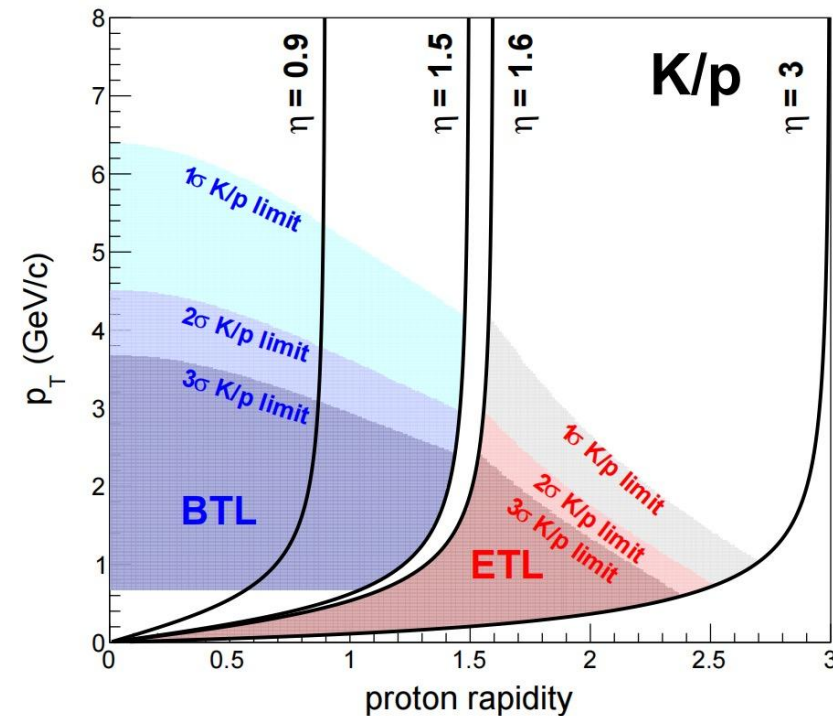
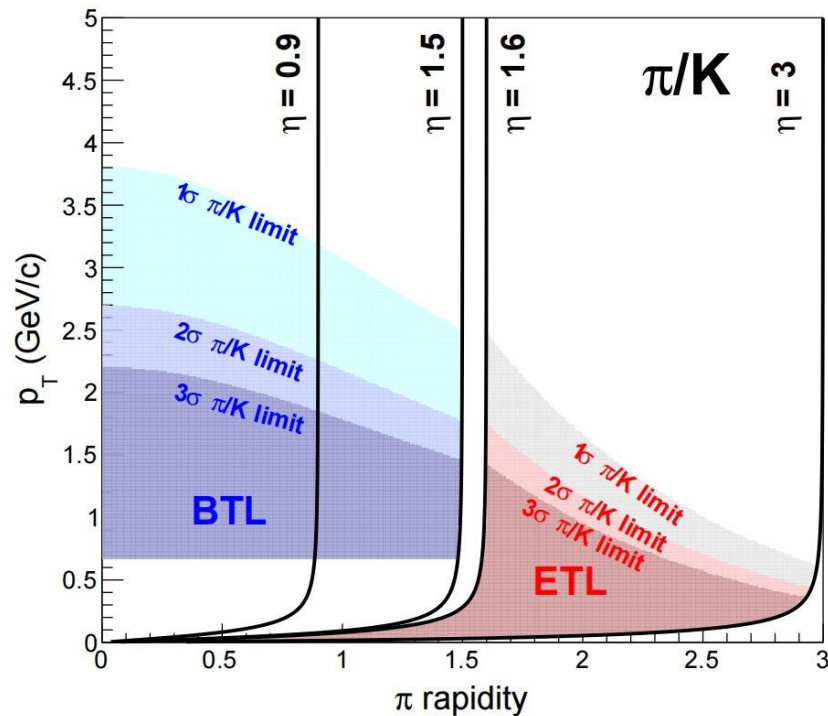
2023.11.16

Outline

1. Introduction of the MIP Timing Detector Project
2. Overview of the ETL
3. Test environment in USTC
4. Test result of single sensor and 15*15 sensors
5. Layout of the new 16*16 probe card and QC plan
6. Summary

Introduction of the MTD Project

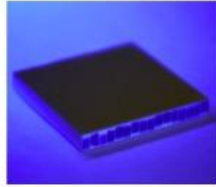
The CMS is going to introduce a new timing detector to measure timing of minimum ionizing particles (MIP) during the High Luminosity LHC (HL-LHC) era. The MIP Timing Detector (MTD) will reduce the effects of up to 200 pileup per bunch crossing, and thus, will provide better reconstruction of particles, and new capabilities for searches for the long-lived particles.



Introduction of the MTD Project

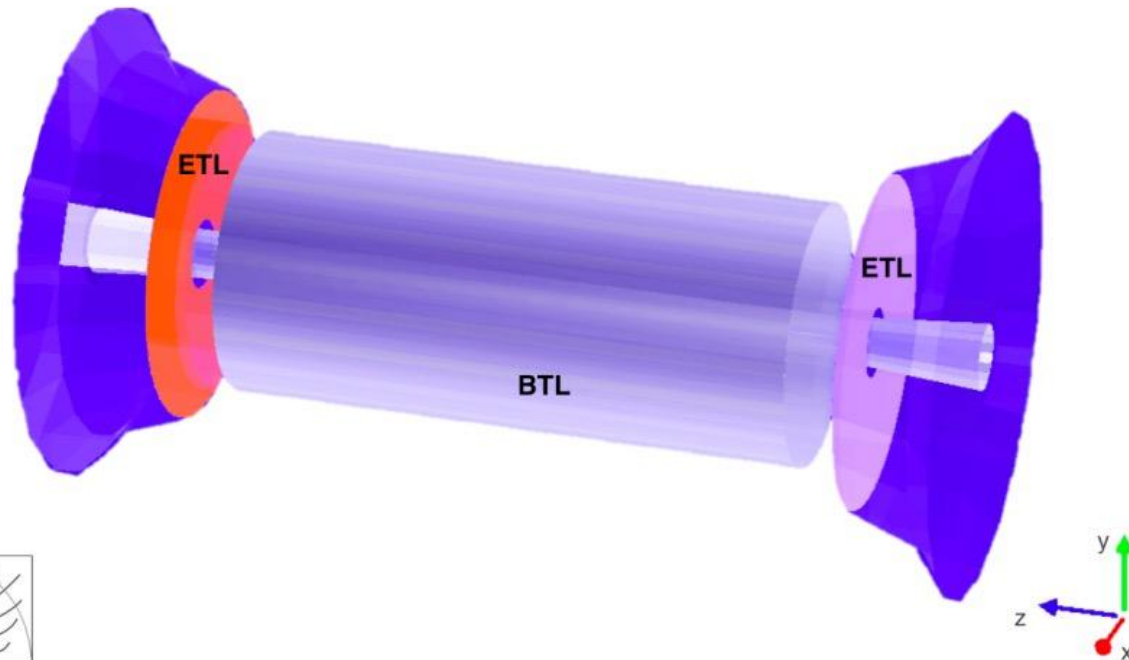
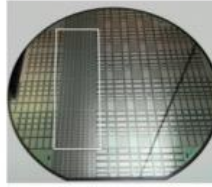
BTL: LYSO bars + SiPM readout:

- TK / ECAL interface: $|\eta| < 1.45$
- Inner radius: 1148 mm (40 mm thick)
- Length: ± 2.6 m along z
- Surface ~ 38 m²; 332k channels
- Fluence at 4 ab^{-1} : $2 \times 10^{14} n_{\text{eq}}/\text{cm}^2$



ETL: Si with internal gain (LGAD):

- On the CE nose: $1.6 < |\eta| < 3.0$
- Radius: $315 < R < 1200$ mm
- Position in z: ± 3.0 m (45 mm thick)
- Surface ~ 14 m²; ~ 8.5 M channels
- Fluence at 4 ab^{-1} : up to $2 \times 10^{15} n_{\text{eq}}/\text{cm}^2$



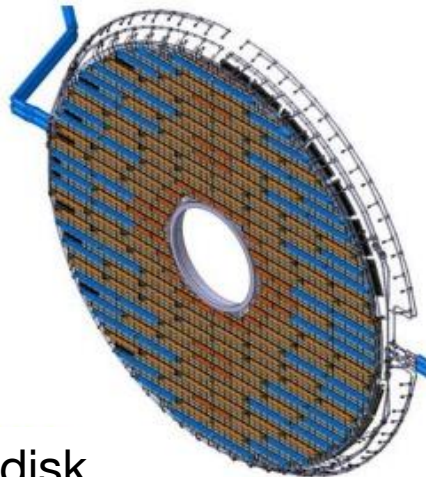
A schematic view of the GEANT geometry of the timing layers for simulation studies comprising a barrel layer (grey cylinder), and two silicon endcap (orange and light violet discs) timing layers in front of the endcap calorimeter.

Overview of the ETL

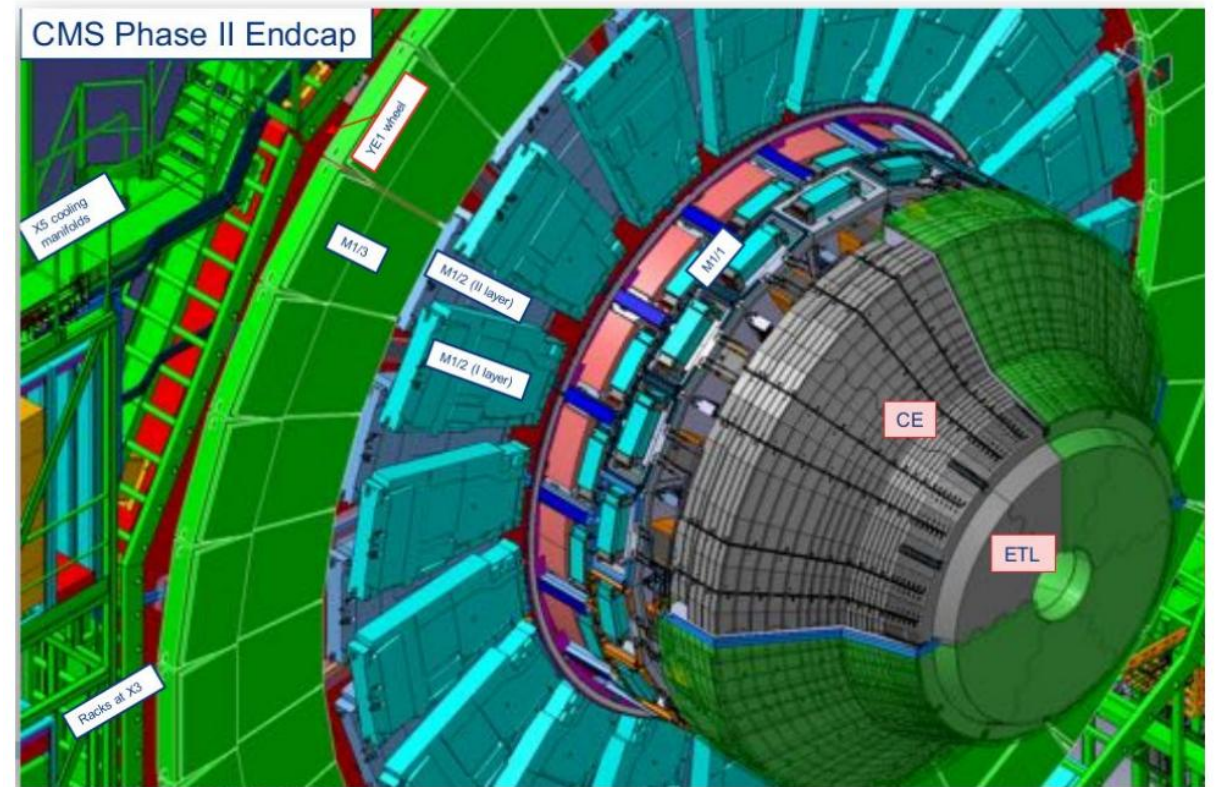
Coverage:

- $z = 3 \text{ m}$ from pp interaction
- $0.315 \text{ m} < R < 1.2 \text{ m}$
- Surface $\sim 14 \text{ m}^2$

Endcap Timing Layer (ETL) will be mounted on the nose of the CMS CE calorimeter



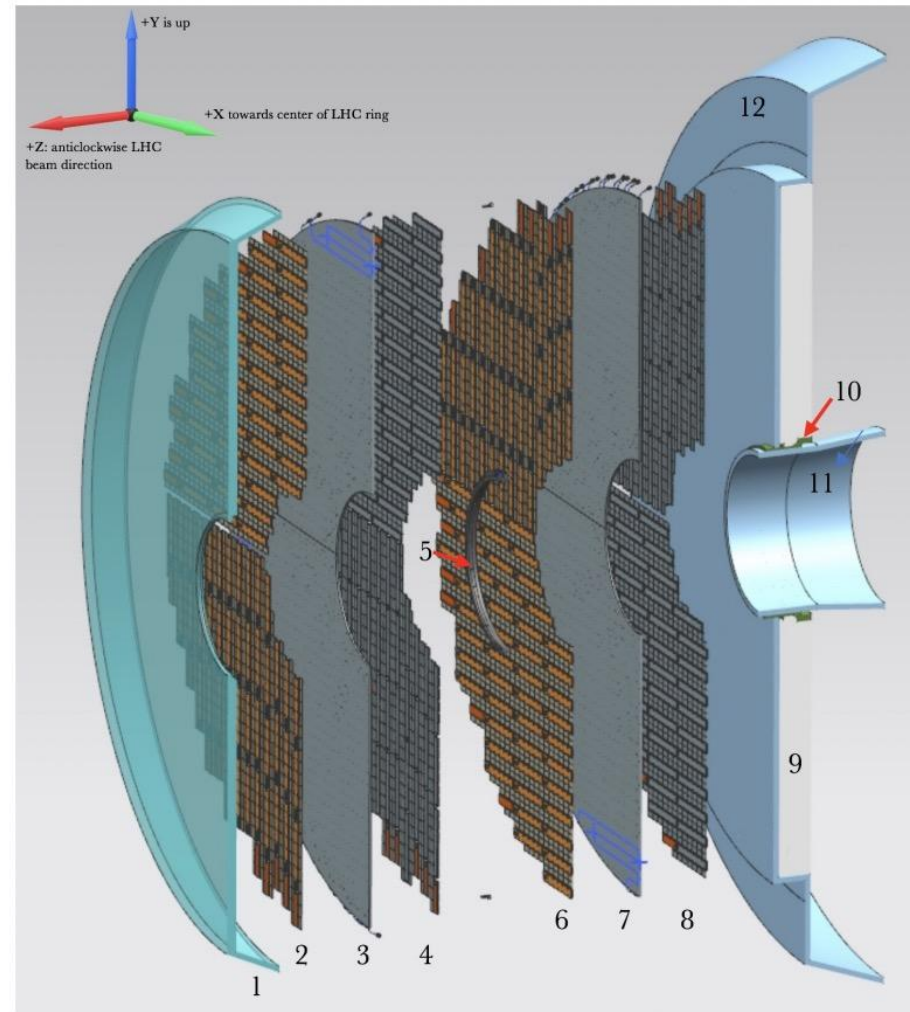
ETL disk



Overview of the ETL

2 double-sided disks for each side

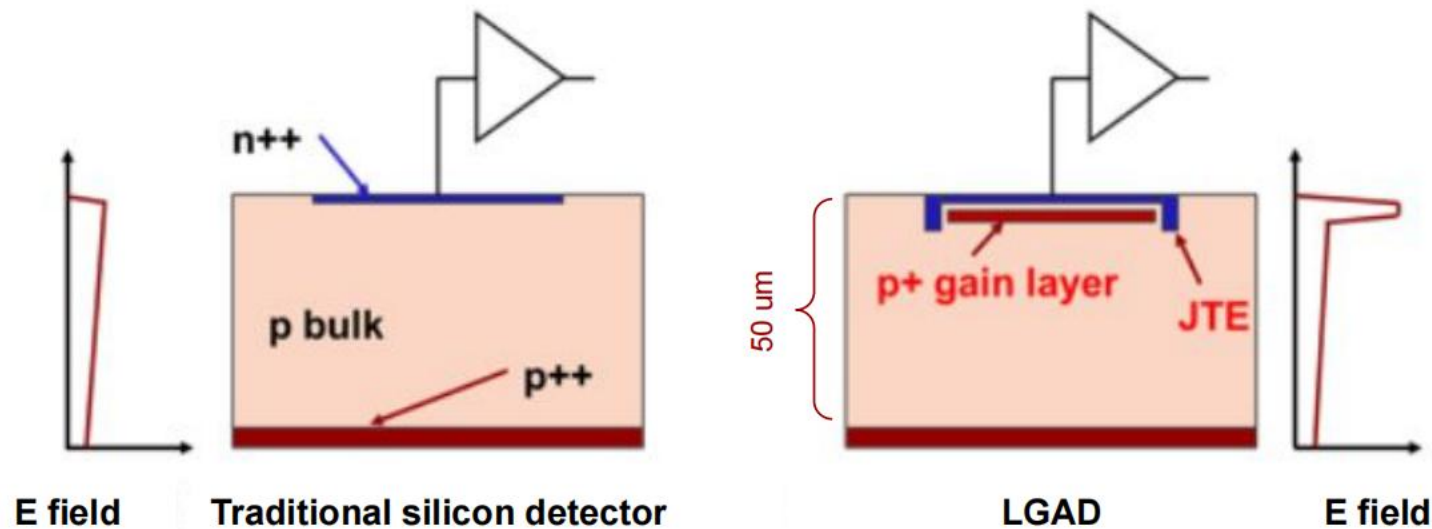
- double-sided disk → large geometrical acceptance
- 2 disks to achieve target time resolution:
 - Single hit resolution < 50 ps
 - track resolution < 35 ps



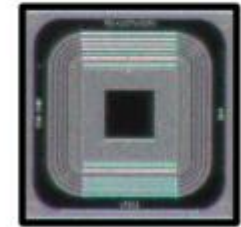
- 1: ETL Thermal Screen
- 2: Disk 1, Face 1
- 3: Disk 1 Support Plate
- 4: Disk 1, Face 2
- 5: ETL Mounting Bracket
- 6: Disk 2, Face 1
- 7: Disk 2 Support Plate
- 8: Disk 2, Face 2
- 9: HGCal Neutron Moderator
- 10: ETL Support Cone
- 11: Support cone insulation
- 12: HGCal Thermal Screen

LGAD sensors for ETL

- ETL will be instrumented with thin (50 μm) silicon sensors based on the Low-Gain Avalanche Diode (LGAD) technology
- Thin sensor + LGAD technology \rightarrow excellent timing performance

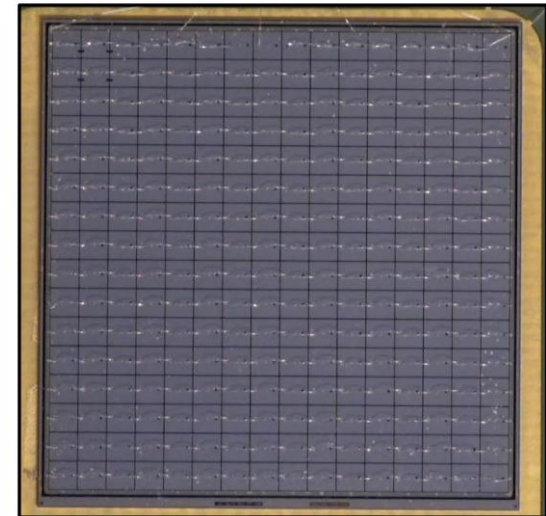


single



evolved during
the past few years

16x16

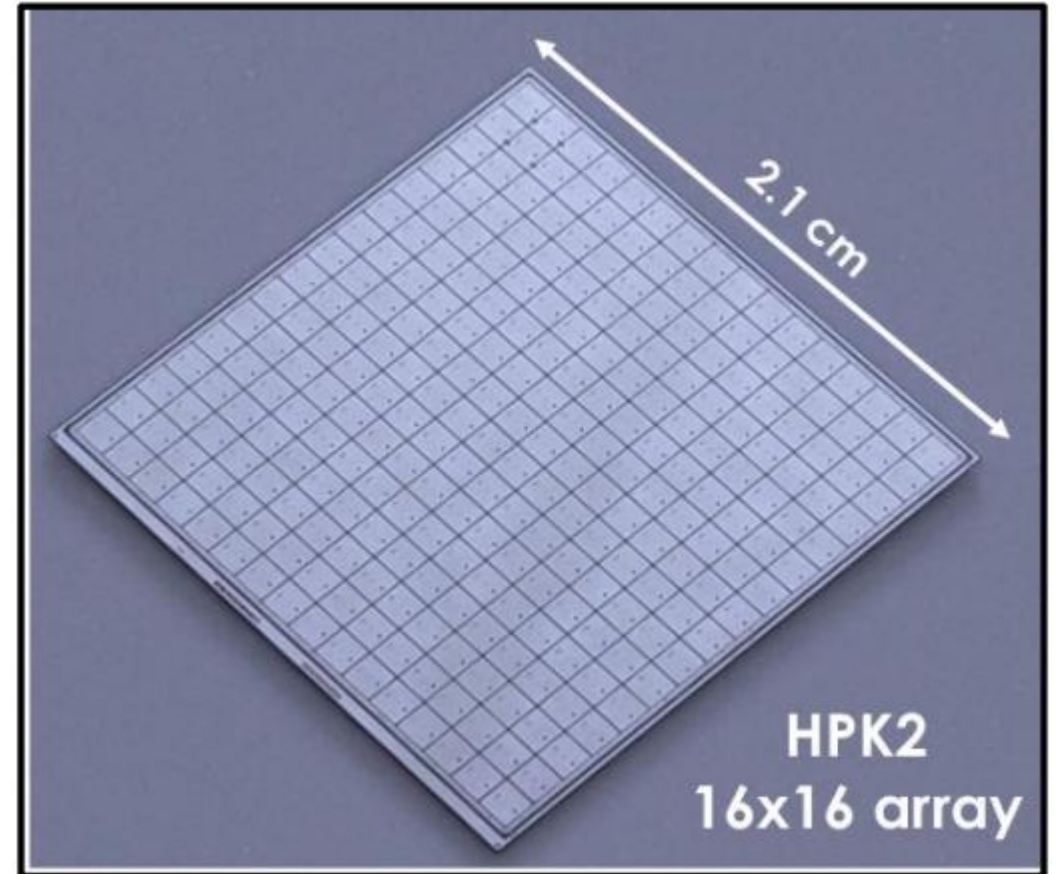


LGAD sensors for ETL

The final ETL sensor will be a 16x16 LGAD, to be bump-bonded to the ETL read-out chip (ETROC)

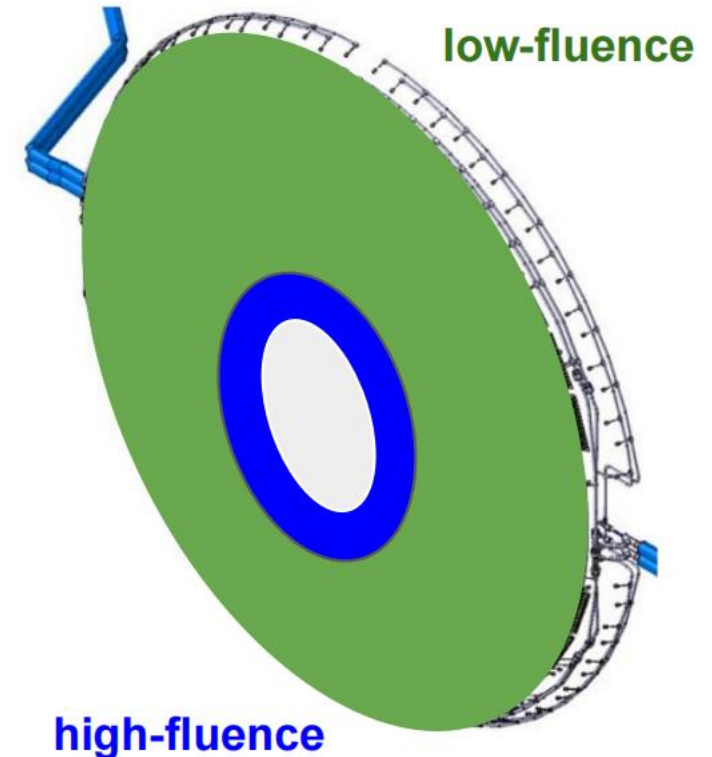
- 1.3 x 1.3 mm² pads for a total surface of 21.4 x 21.6 mm²
- From the beginning to the end of HL-LHC lifetime, sensors are expected to:
 - achieve time resolution < 50 ps
 - deliver > 8 fC

ETL sensors need also to be radiation-hard to survive the harsh radiation environment @ HL-LHC → LGADs suited for this, as they proved to be able to withstand high radiation fluences

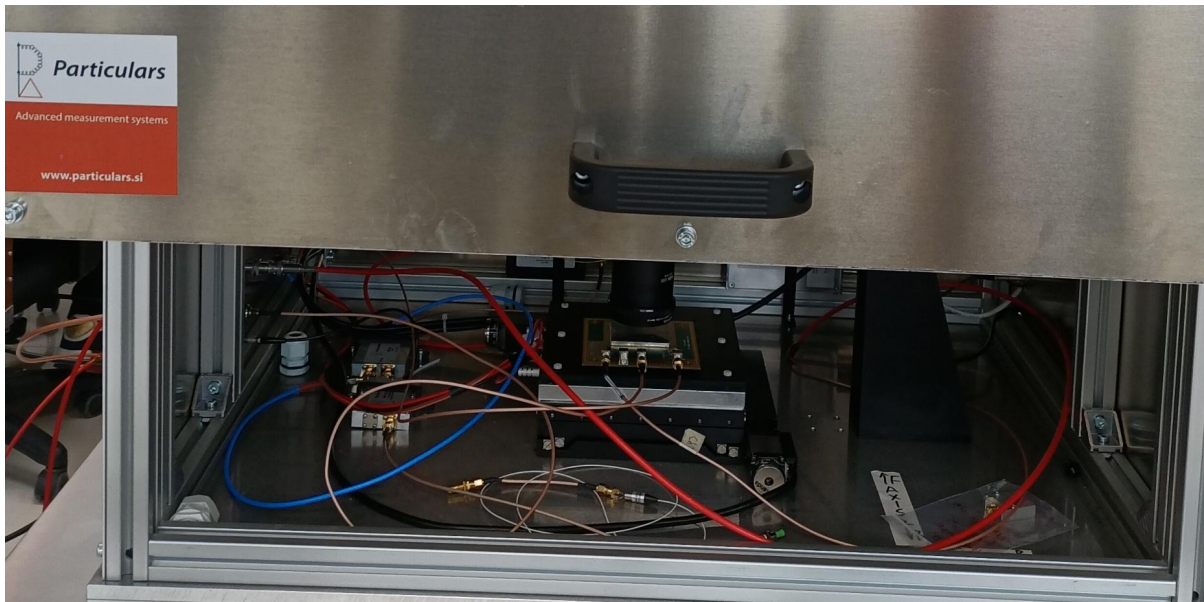


LGAD sensors for ETL

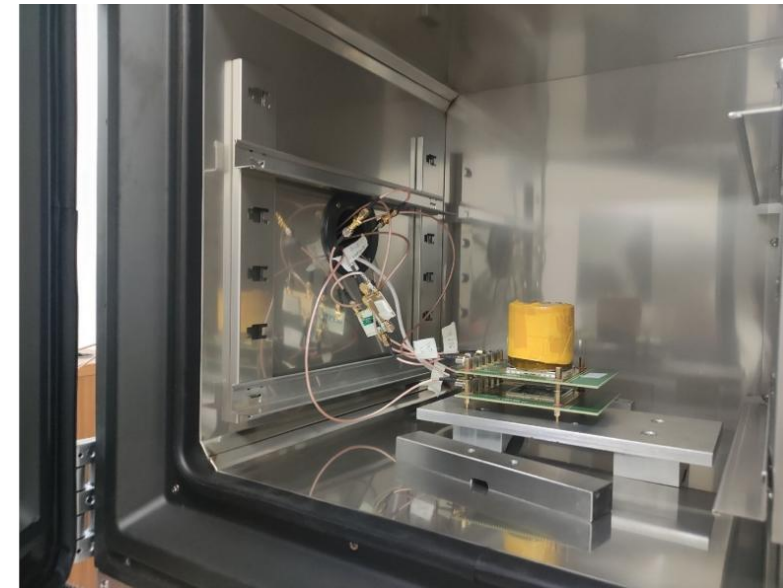
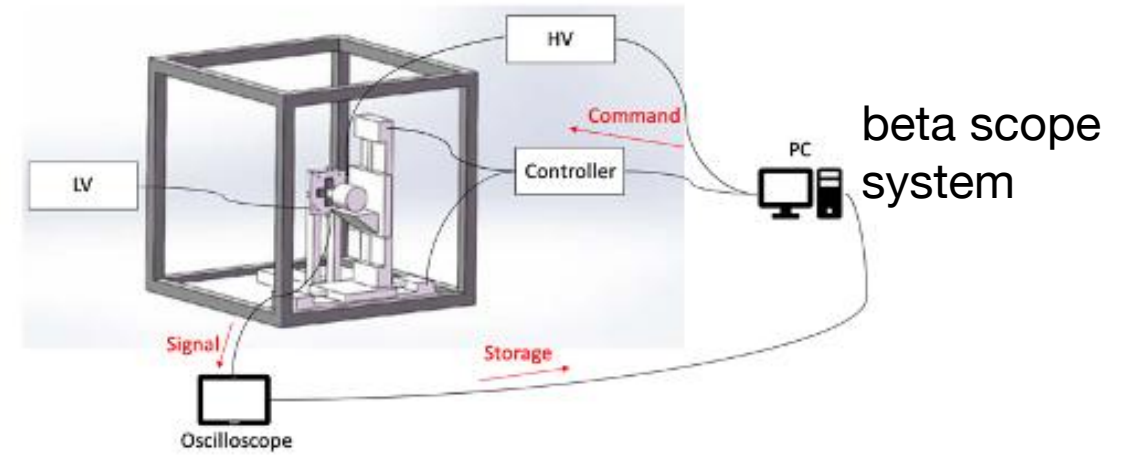
- Irradiation in ETL won't be uniform, but will have a radial dependence
- The fluence received by sensors at the end of the detector lifetime defines the so-called high- and low-fluence areas onto the disks:
 - low-fluence area ($\Phi \leq 1e15$ neq/cm²), ~85% of the disk
 - high-fluence ($1e15$ neq/cm² < $\Phi \leq 1.5e15$ neq/cm²), ~15% of the disk
- The $1e15$ neq/cm² threshold is set as it represents the turning point in terms of LGADs performance degradation
(Φ expressed in 1 MeV neutron equivalent)



Test environment in USTC

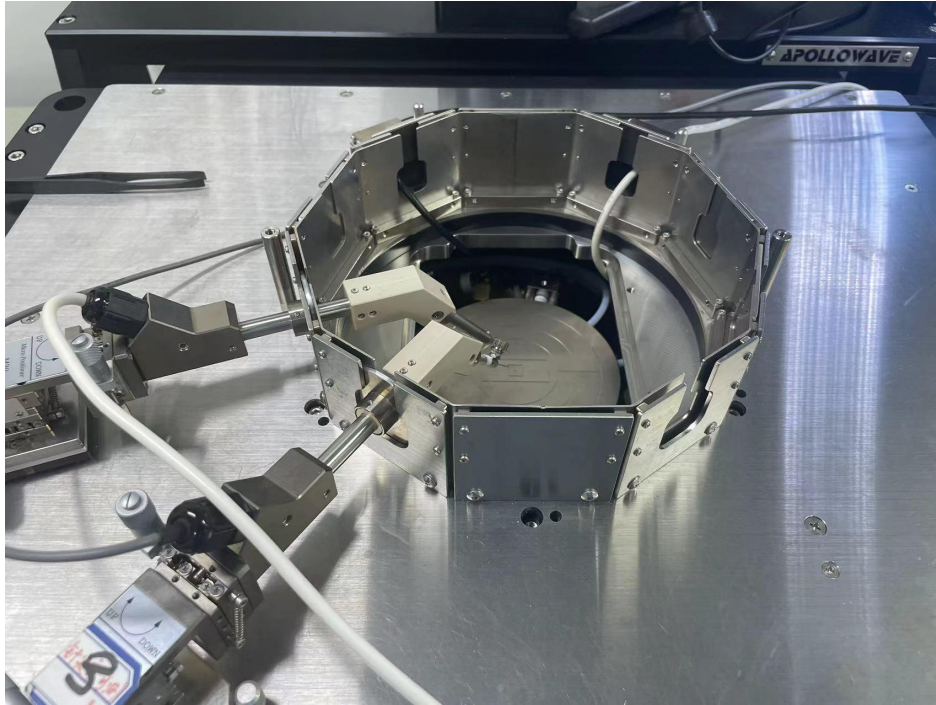


Scanning laser TCT (being assembled)

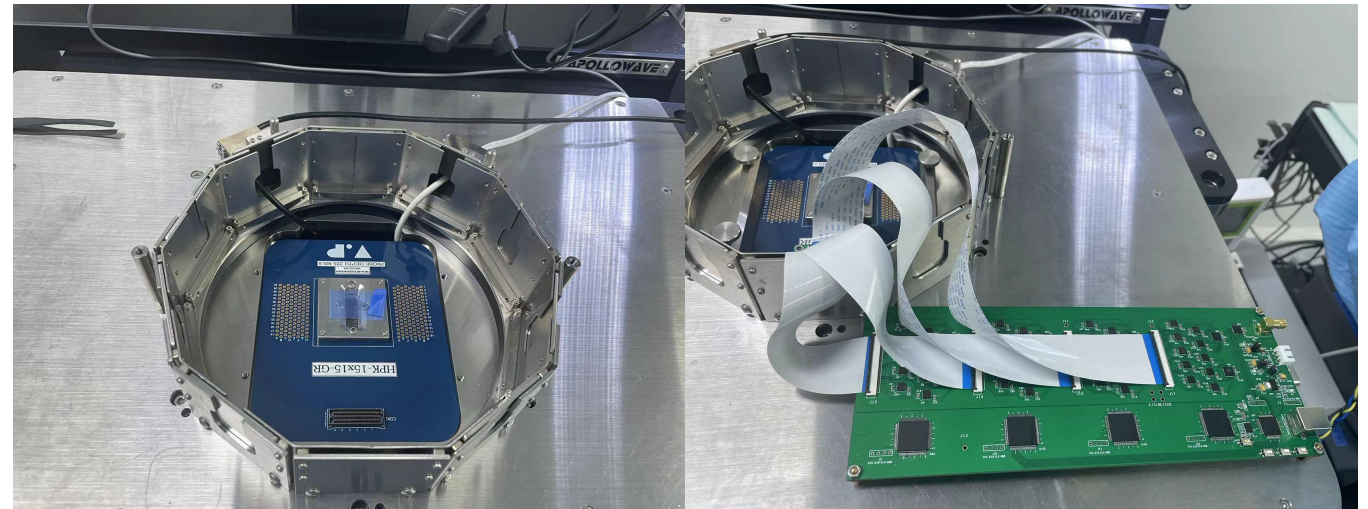


Environmental chamber: -70 ~ 180 degree

Test environment in USTC



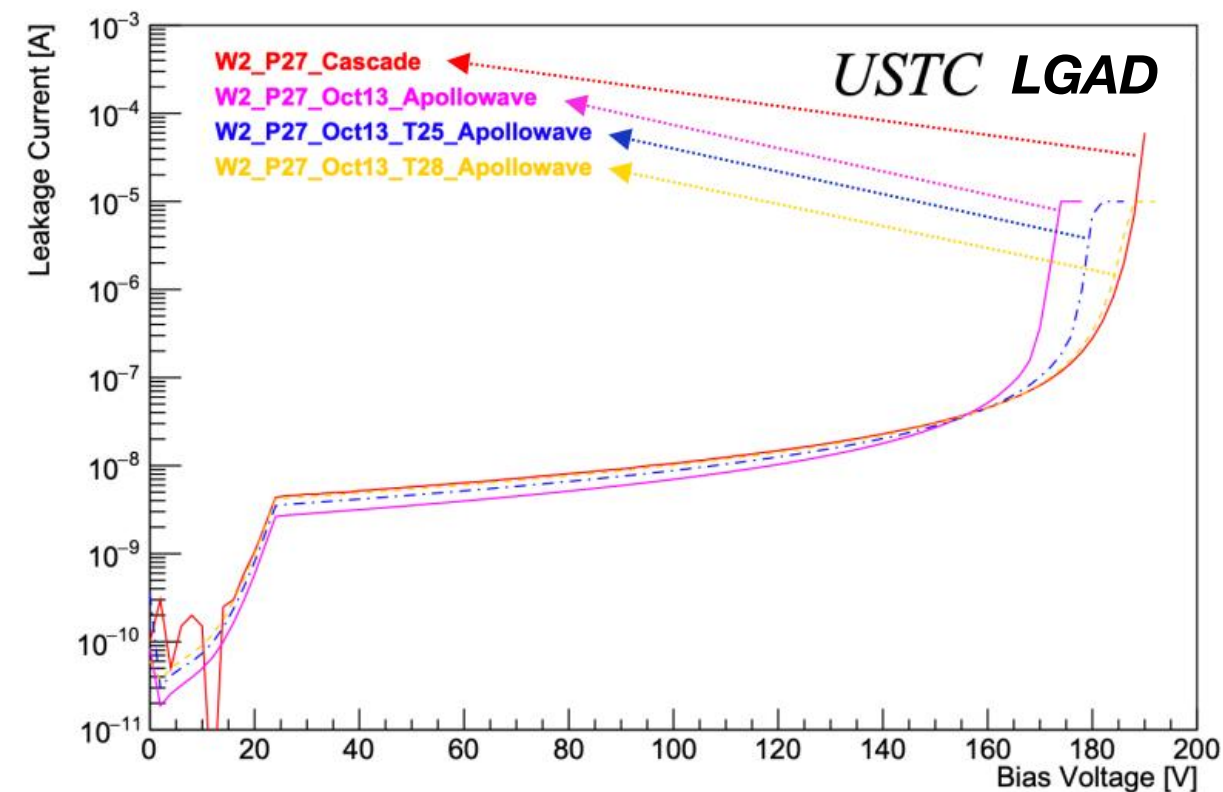
Probe station with up to 5 probes
In clean room, Temperature adjustable



15*15 probe card controlled by FPGA

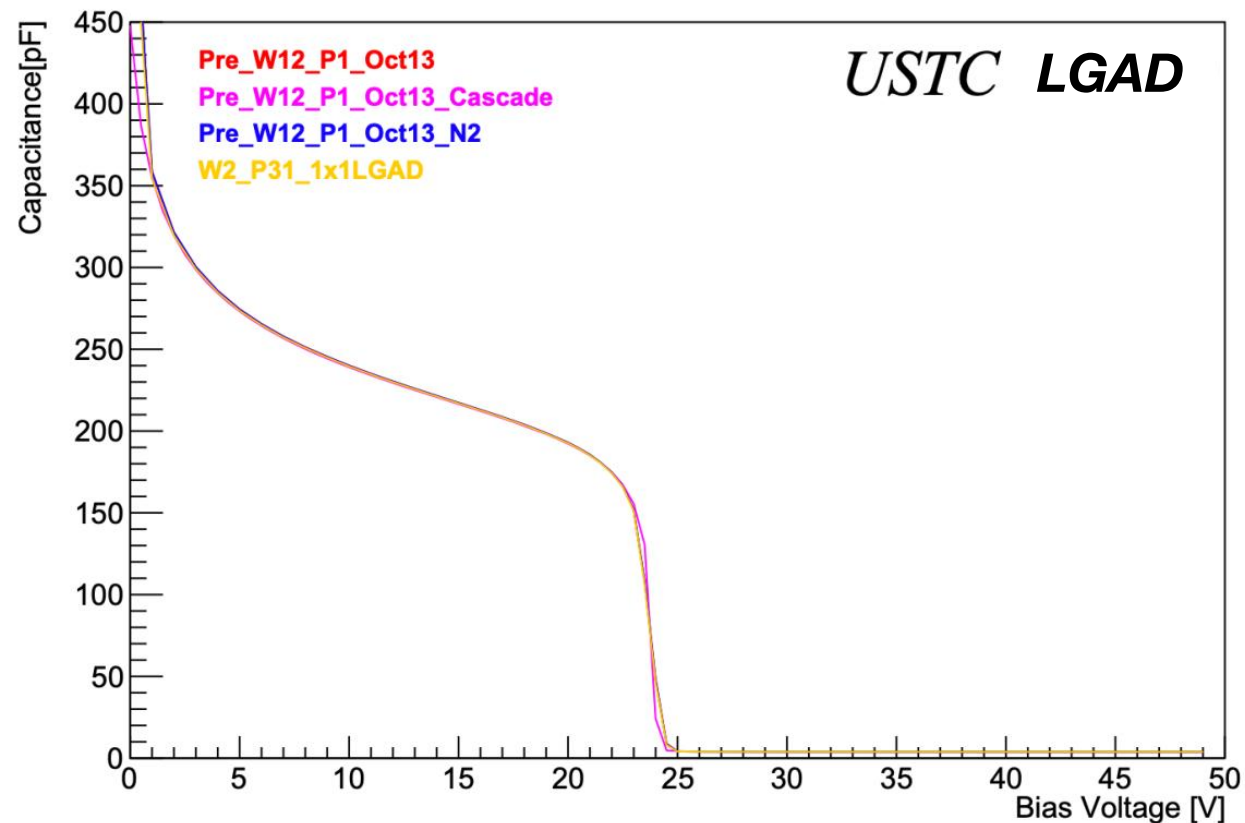
Test result, 1*1

labprob-Data-IV-2023Jul19-USTCIMEPre-1x1-comparison-P27-Steady [Log]



IV test result

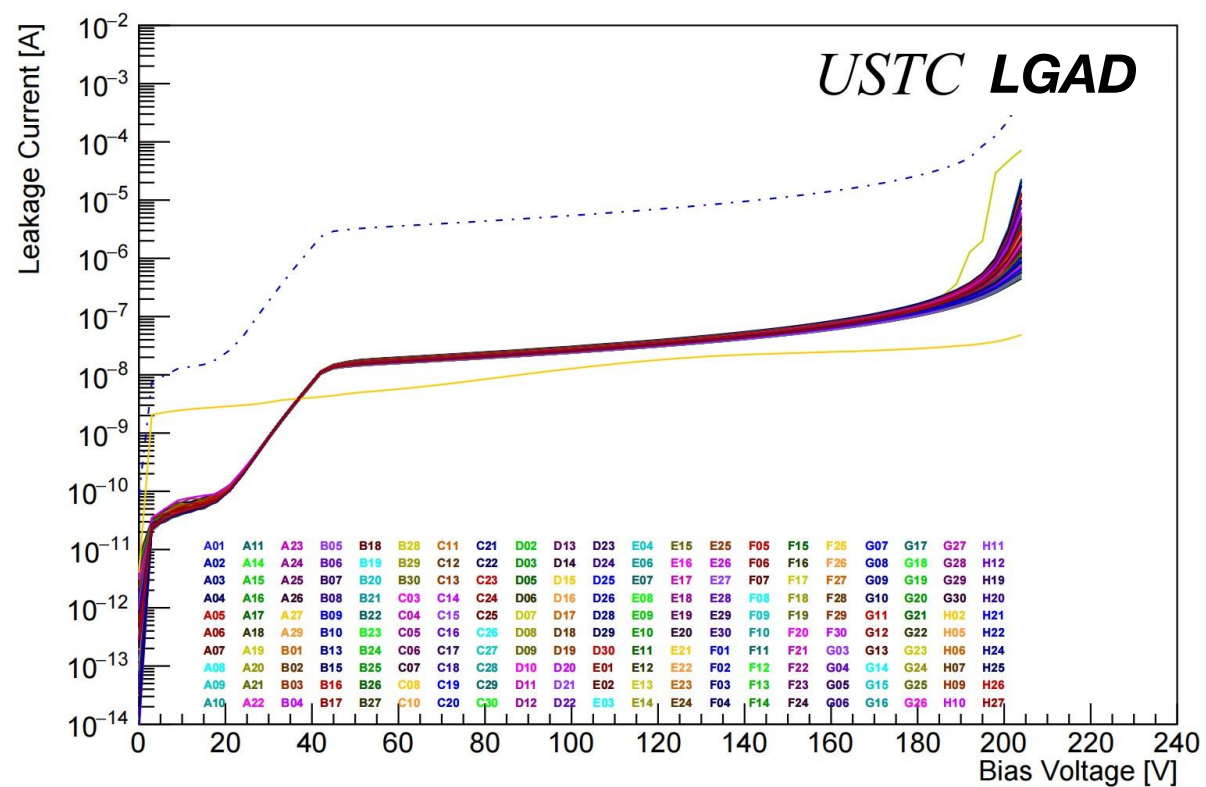
labprob-Data-CV-2023Mar16-USTC1x1-show [Linear]



CV test result

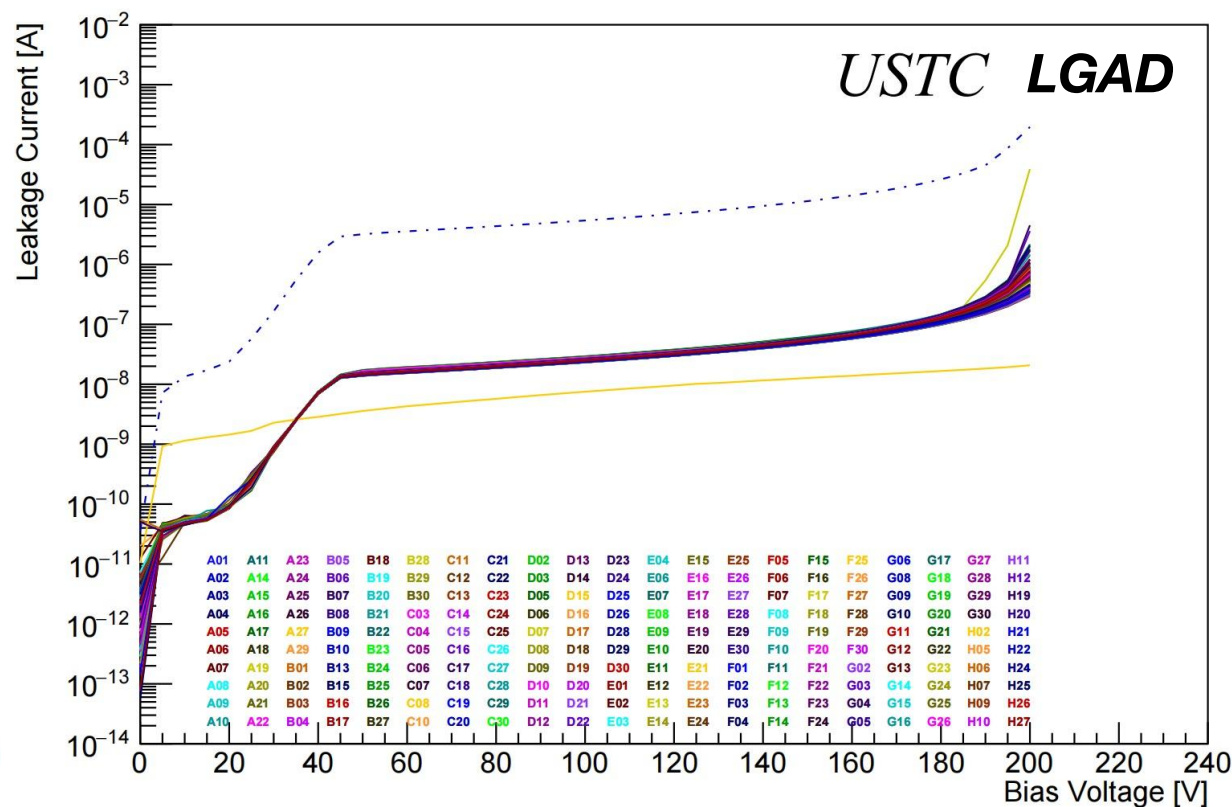
Test result, 15*15, IV

labprob-Data-IV-2022Apr15-USTC15x15-0E0-W20-P47_SE4-IP7 [Log]



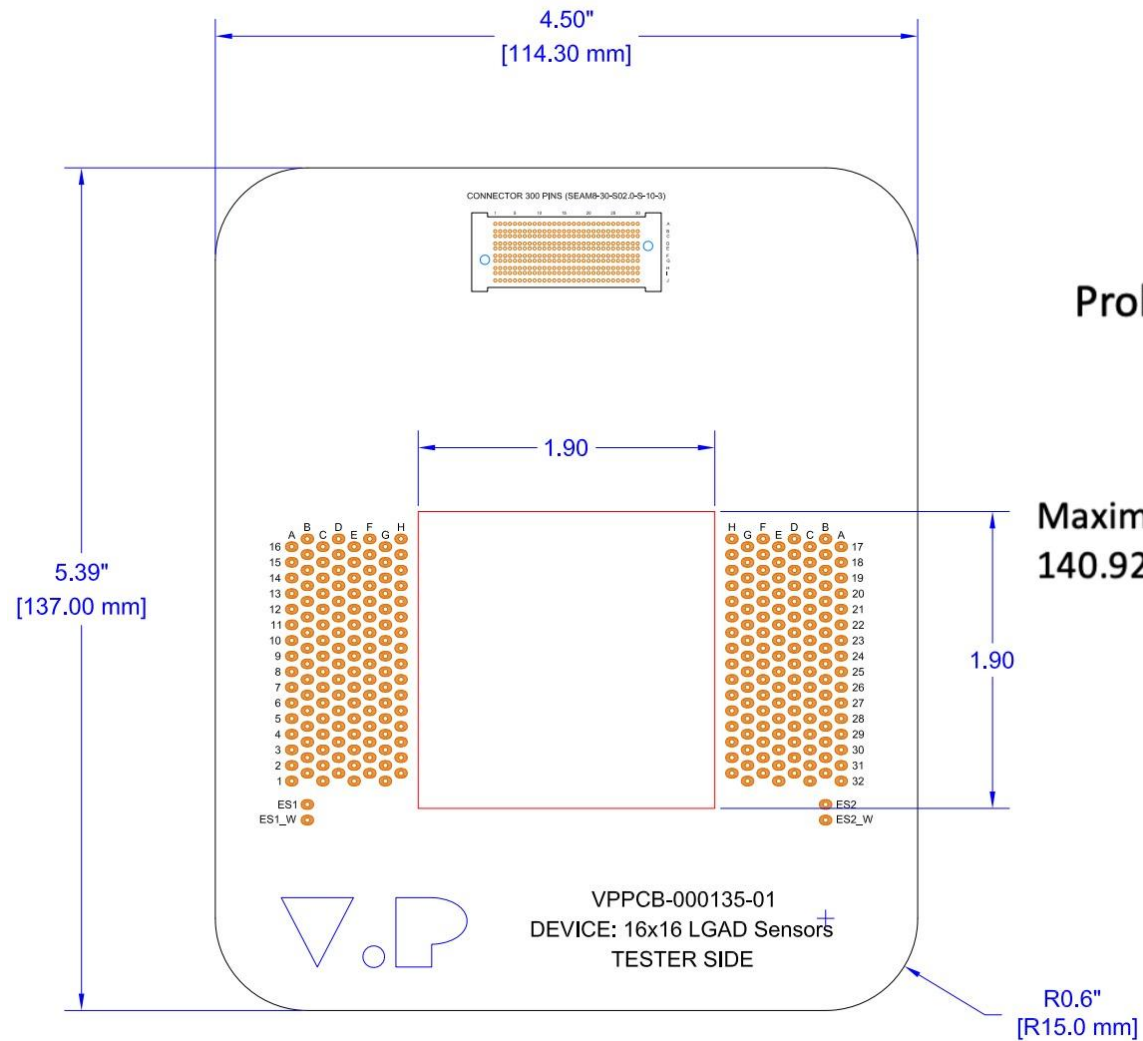
The old testing result

labprob-Data-IV-2023Jul19-USTCIMEv2.1-15x15-W20_P47-Fullscan_N2 [Log]



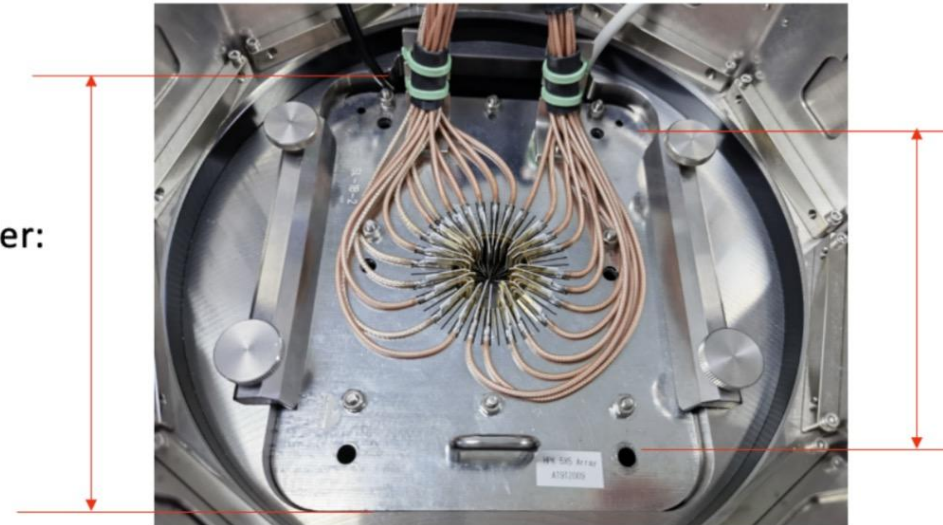
The new testing result

Layout of the 16*16 probe card



Probe-card holder:

Maximum length of probe holder:
140.92 mm (5.54 inch)

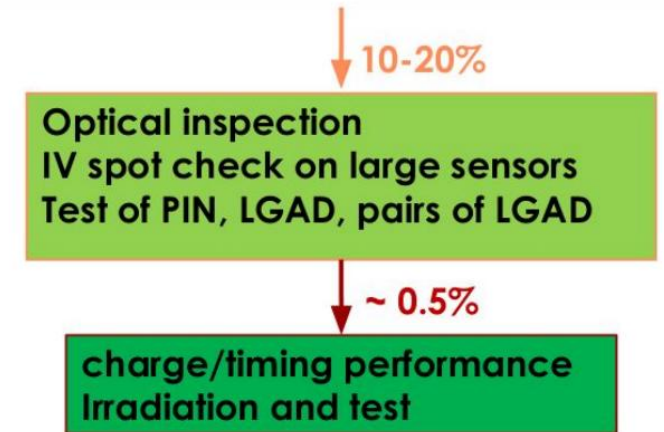


Sensor QC plan

Quality control(QC) will start after quality assurance(QA) and post-wafer process

On 16x16 sensors:

- Optical inspection (chipping, scratches, other)
- Re-measure IVs cross-checking the vendor quality maps
 - monitor current and breakdown voltage after processing
 - spot “bad” pads not present on-wafer
- measurements of timing performance (with beta setup) of pre-rad / irradiated samples



to be performed at ETL testing sites

Summary

- The MTD project are progressing well. USTC will undertake sensor testing work.
- The repeated test result looks good. We are ready to test the new LGAD sensor.
- Radiation resistance testing will be conducted afterwards.
- After QA and post-wafer processing, the QC will start.