FOCAL-E Pixel Layer SystemC Simulation

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Outline

- **Introduction**
  - FOCAL-E Pixel Layer
  - SystemC Framework

- **Link Saturation**
  - Data rate per link
  - Duration of Link Saturation

- **Busy Violation**
  - ALPIDE Trigger and Strobe Scheme
  - Principles of Busy Violation
  - Busy Violation rate per chip
  - Duration of Busy Violation
  - Solution for Busy Violation

- **Summary**

➢ **Location**

◆ located 7m away from the IP(Interaction Point) ,slightly inside the L3 door.

>>Should be located close to the beam, far from the interaction point(IP)

>>The compensator magnet poses a upper limit to the furthest location from IP available for FoCal installation

>>3.4 < η < 5.5 over the full azimuthal coverage(pseudorapidity)

➢ **Composed by three different technologies**

◆ **Electromagnetic calorimeter**(Pad and pixels sensors)

FOCAL-E PAD

- 18 layers of silicon pad sensors of 9 x 8 cm^2
- Pad size 1 cm^2
- Readout with HGCROC v2(High Granularity Calorimeter ReadOut Chip)

FOCAL-E Pixel

- 2 ALPIDE pixel layers
- Monolithic active pixel sensors(MAPS) with pixel size of ~30 x 30 μm^2

◆ **Hadronic calorimeter**(Copper/fibers)

- 9 Cu-scintillating fiber blocks
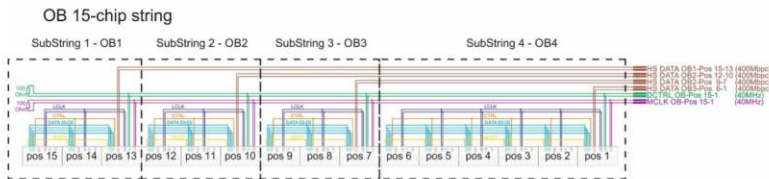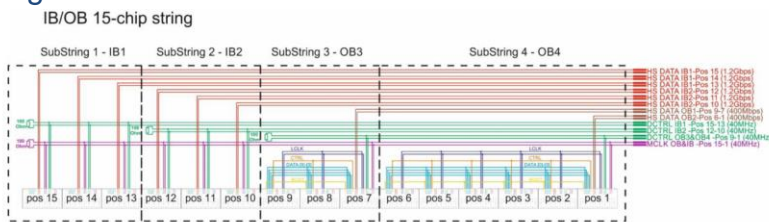- Block size ~ 6.5 x 6.5 cm2
- Length ~110 cm
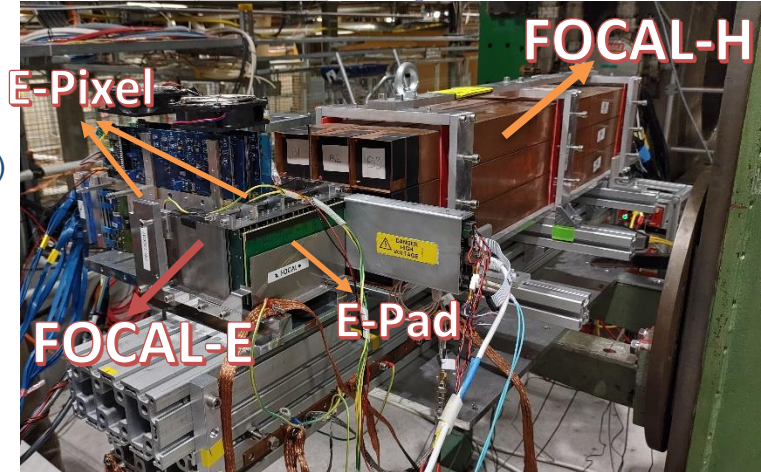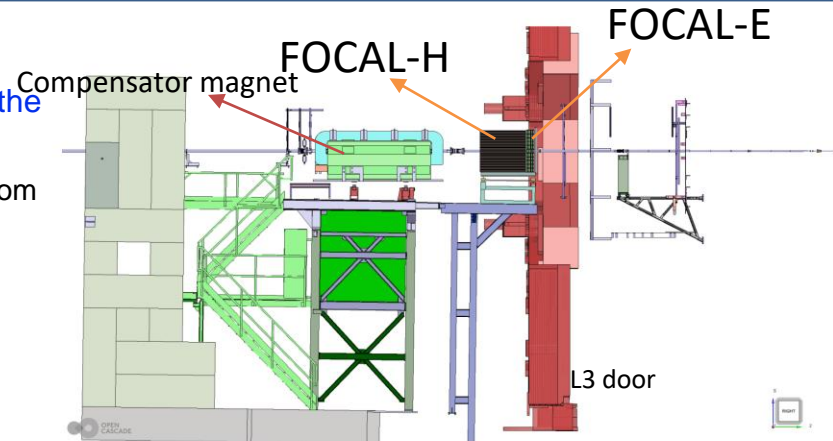
➢ FOCAL-E Model

• **The FoCal-E is made of 20 layer**

18 instrumented with Si-PAD and two (the 5th and the 10th) with Si-Pixel detectors

2 PAD&Pixel segments and 3 Pad segments form a module.

Stacking 2 × 11 of them makes the two half detectors
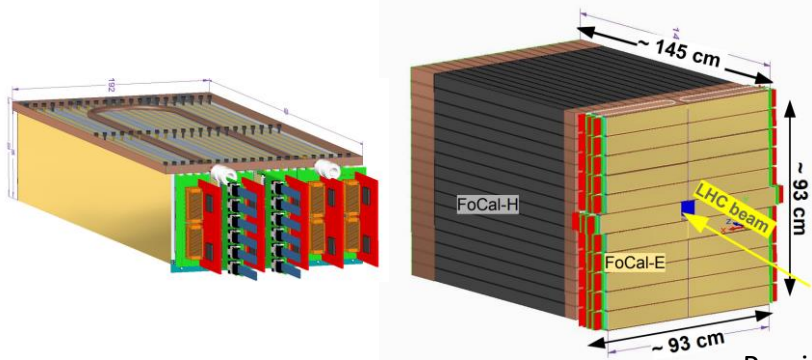
Previous

Multi-chip strings
Previous design:2 types
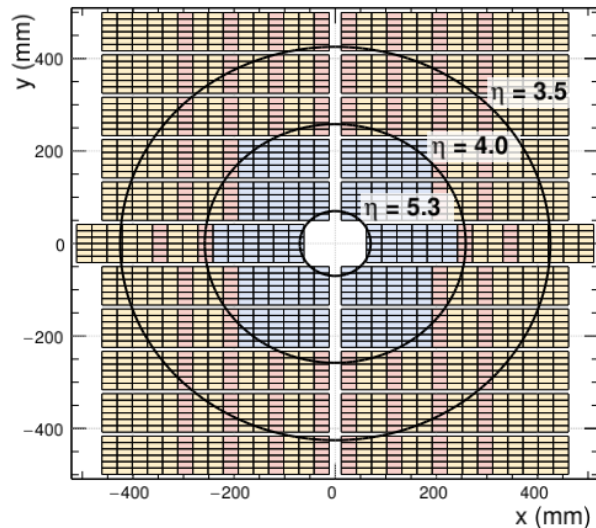the IB/OB 15-chip string
the OB 15-chip string

Latest design:3 types(August 31, 2023**)**
the IB/OB 15-chip string
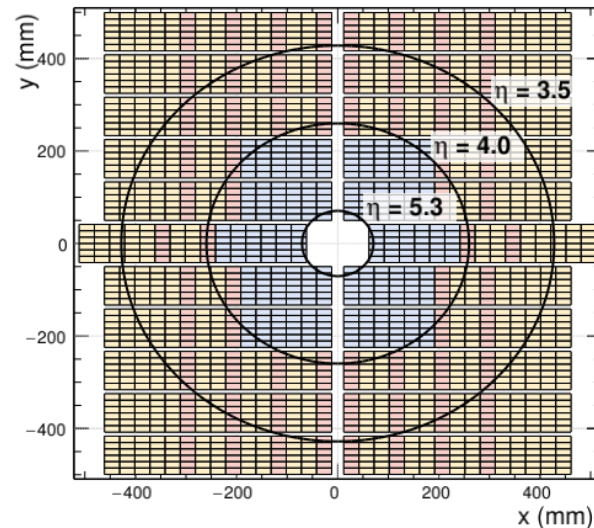the OB 15-chip string
the IB/OB 12-chip string

FOCAL-E Pixel Layer

FoCal-E Pixel Layer 5 Simulation Chip Modes

FoCal-E Pixel Layer 10 Simulation Chip Modes

Blue: inner mode chips
Red: outer mode master chips
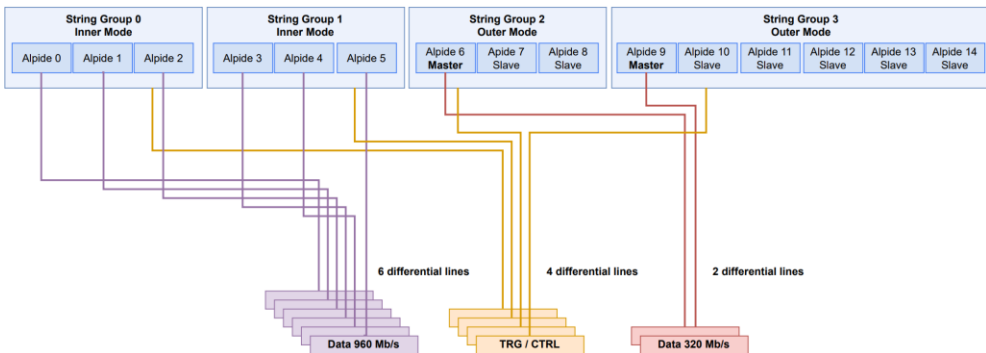Yellow: outer mode slave chips

- Pixel layers at FoCal-E Layer 5 and 10

- The detector consists of 22 patches per layer each with 6 pixel strings.

- Each pixel string contains 15 ALPIDE chips
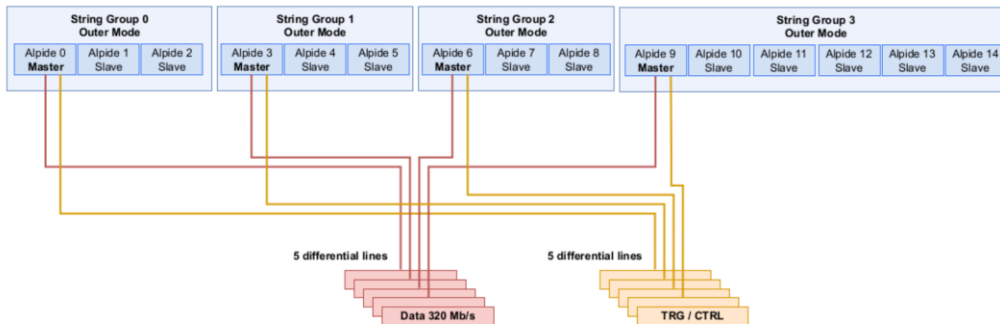
- 1980 ALPIDE(Alice Pixel Detector) chips per layer

➢ **String Models in Current SystemC model**

Inner string, 15 alpides

4 x 15 Focal_I3_I3_O3_O6 strings per layer
2 x 4 x 15 x 6 inner mode links = 720 links
2 x 4 x 15 x 2 outer mode links = 240 links

Outer string, 15 alpides

4 x 18 Focal_O3_O3_O3_O6 strings per layer
2 x 4 x 18 x 4 outer mode links = 576 links

➤ SystemC Framework Basic Structure

Schematic overview on the functionalities of the FoCal-E Pixel Simulation Framework
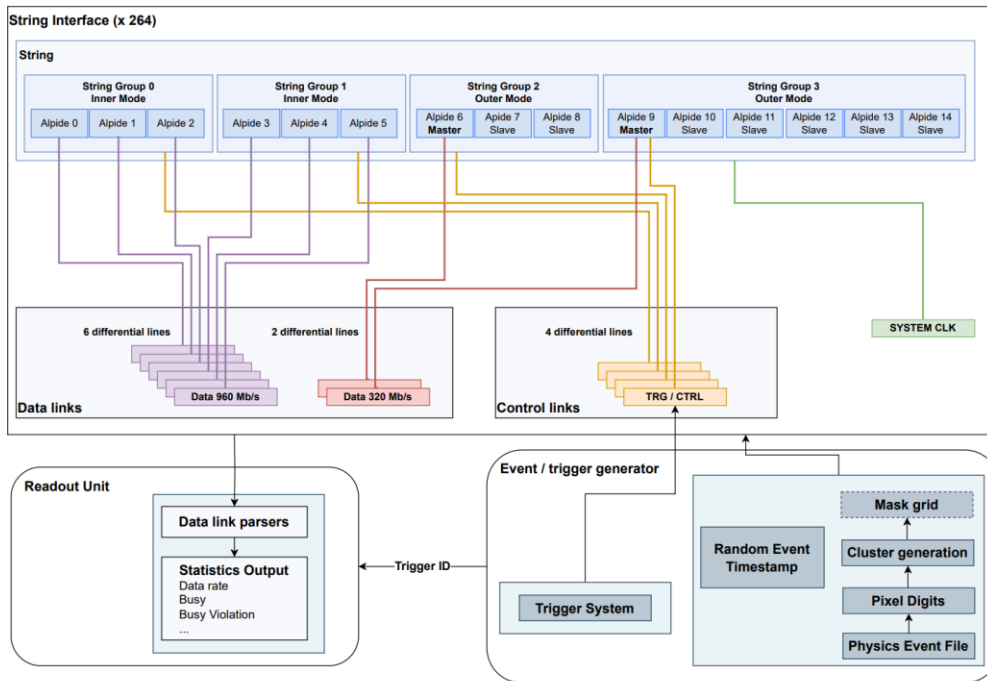
- Input for the pixel hits : simulated minimum bias events(generated with the PYTHIA event generator and processed with FoCal simulation framework)

- The particle hits in the pixel layers are transformed to pixel hits in the chip internal coordinate system
- The **pixel cluster generation** model is applied for the formation of a realistic occupancy.
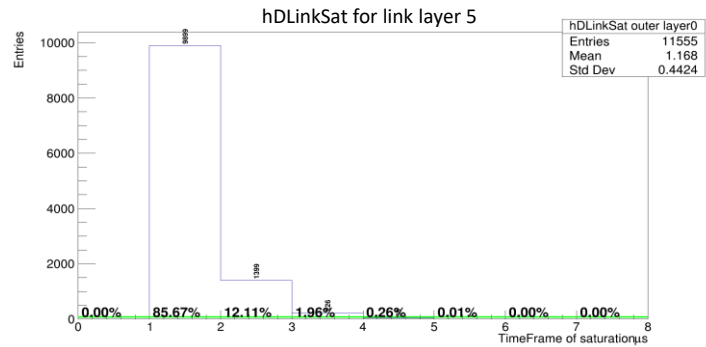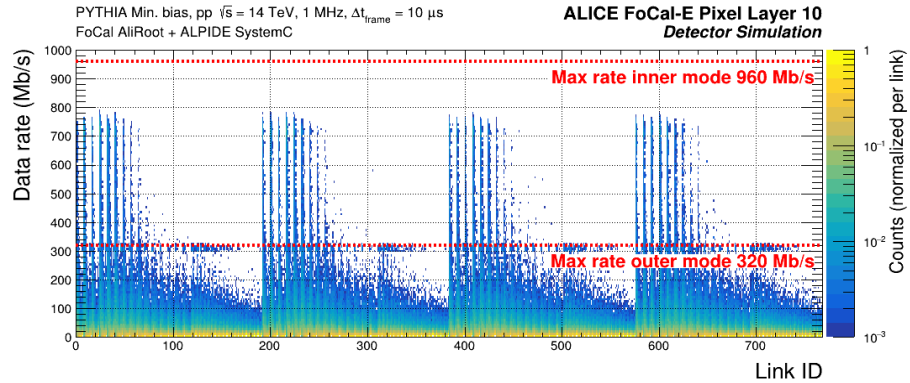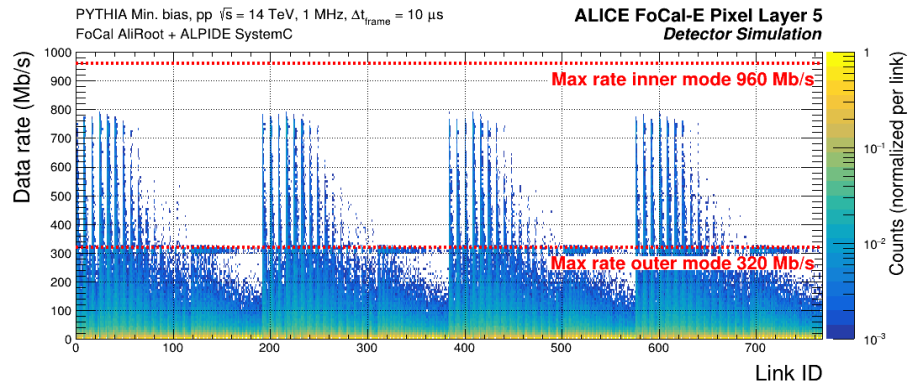
Default

Mean cluster size $\quad n_{cl.size} = 4$

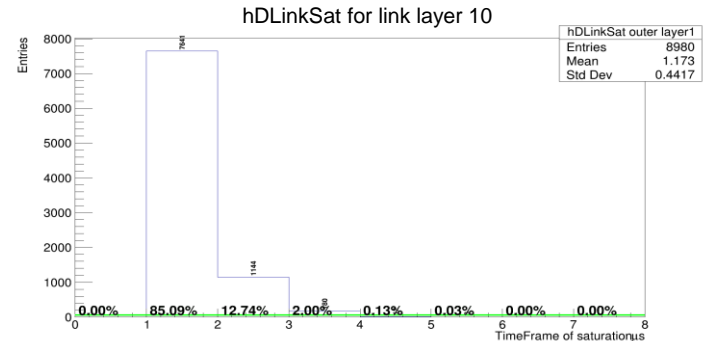Mean cluster width $\sigma_{cl.size} = 1.4$

The core of the framework is the digital simulation in SystemC of 264 pixel strings with 15 ALPIDEs each (here shown for an inner mode string).

Link saturation

PYTHIA Min. bias, pp √s = 14 TeV, 1 MHz, Δt_{frame} = 10 μs
FoCal AliRoot + ALPIDE SystemC

ALICE FoCal-E Pixel Layer 5
Detector Simulation

Max rate inner mode 960 Mb/s

Max rate outer mode 320 Mb/s

hDLinkSat for link layer 5

hDLinkSat outer layer0	
Entries	11555
Mean	1.168
Std Dev	0.4424

0.00% 85.67% 12.11% 1.96% 0.26% 0.01% 0.00% 0.00%

Exceeding 280 Mb/s is considered saturated links
Leaving a buffer of 40 Mb/s between 280 Mb/s and 320 Mb/s

PYTHIA Min. bias, pp √s = 14 TeV, 1 MHz, Δt_{frame} = 10 μs
FoCal AliRoot + ALPIDE SystemC

ALICE FoCal-E Pixel Layer 10
Detector Simulation

Max rate inner mode 960 Mb/s

Max rate outer mode 320 Mb/s

hDLinkSat for link layer 10

hDLinkSat outer layer1	
Entries	8980
Mean	1.173
Std Dev	0.4417

0.00% 85.09% 12.74% 2.00% 0.13% 0.03% 0.00% 0.00%

1 frame is the highest(approximately85%)
2 frames at 12%

The inner data rate on the inner links will be operated with good margin (> 10%) to the full link speed
The outer mode links are simulated to run occasionally on full bandwidth of 320Mbps after having been hit by an high occupancy event.
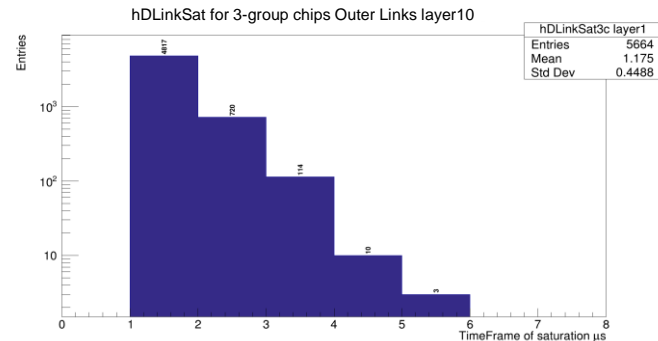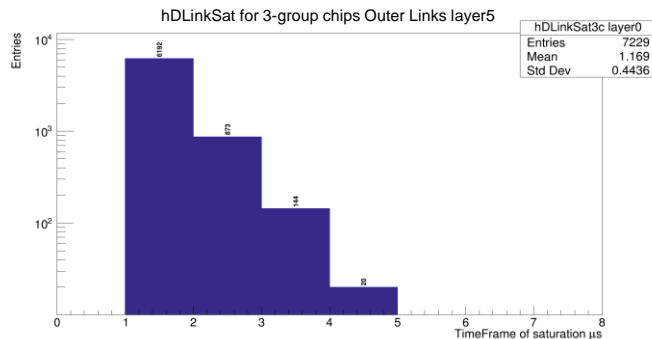
The proportion of saturated 3-group outer chips to the total outer chips:

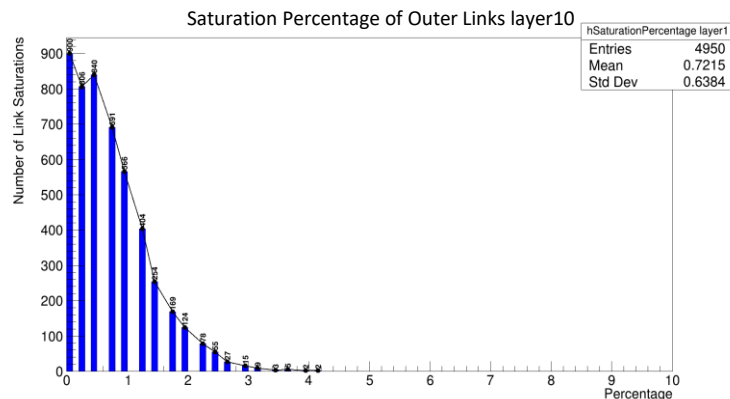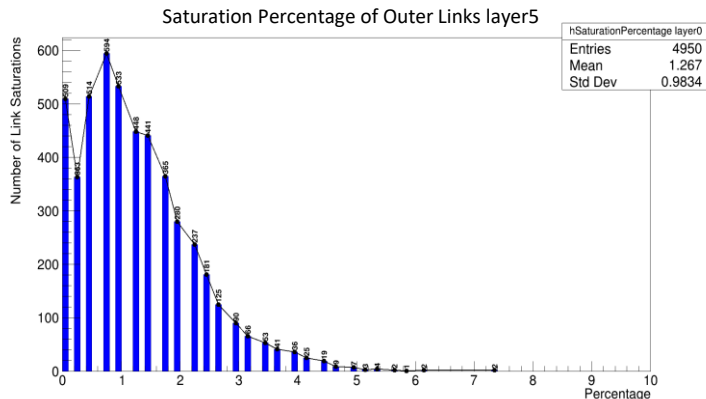$$\frac{\sum t_{frame} \times N_{3-group.sat}}{\sum t_{frame} \times N_{tot.sat}}$$

Layer 5:   8450/13600=62.1%
Layer 10:   6654/10532=63.2%

3-group chips are more prone to saturation
Average duration of saturation is higher than that of 6-group chips

3-group chips outer link saturation duration

Layer 5   ≈ 1%
Layer 10 < 1%

The percentage of saturated Outer links out of the total Outer links each time.

Store up to 3 pieces of data
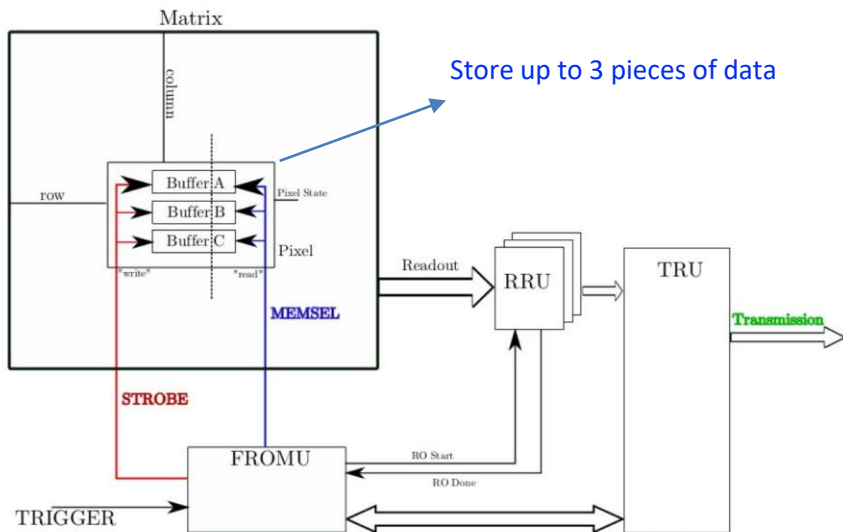
Frame and ReadOut Management Unit(FROMU):
controls the framing and readout in the chip
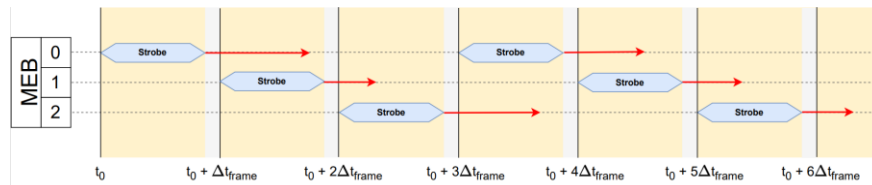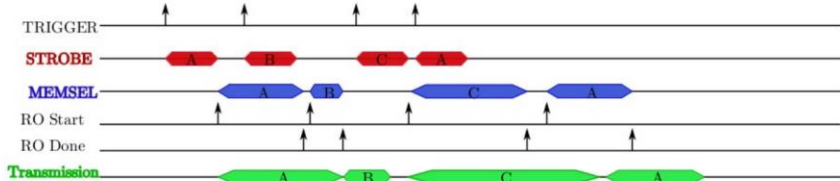keeps track of which buffers of the MEB are in use

Region Readout Unit (RRU):
readout of pixels from its region in the pixel matrix into a region FIFO

Top Readout Unit (TRU):
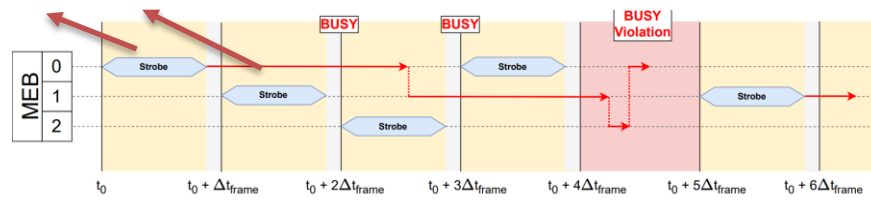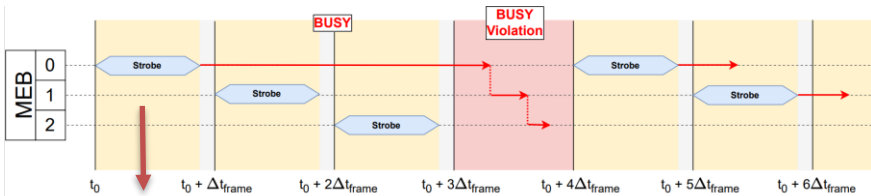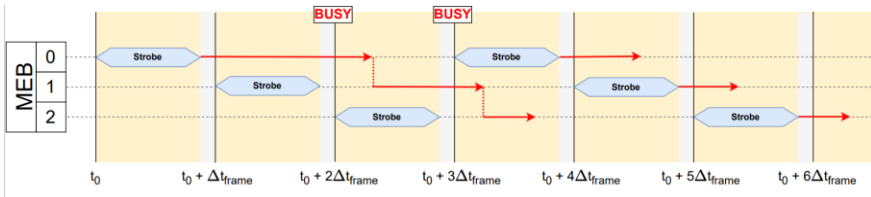Readout from the FIFOs of the RRUs
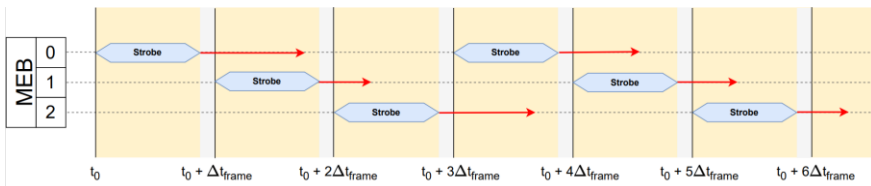framing of the data

3-line global signal

STROBE: latch a hit into the current Hit Storage Latch
MEMSEL: read from the latches

continuously triggered mode(Default)

$$f_{trigger} = 100\text{k}Hz$$

$$\Delta t_{frame} = \frac{1}{f_{trigger}} = 10\mu s$$

- When the pixel is active during the opening of the strobe window, the pixel hit is latched into the Multi-Event Buffer (MEB) and remains there stored until the matrix readout of the event has started.

BUSYV happen in the pixel matrix / RRU and the "slow" pixel readout (50ns/pixel)

- High occupancy events
- Not dominated by data link speed

When the trigger rate is faster than readout rate

Busy Flag:
The pixel hits are being latched to the last free position in the MEB

Busy Violation:
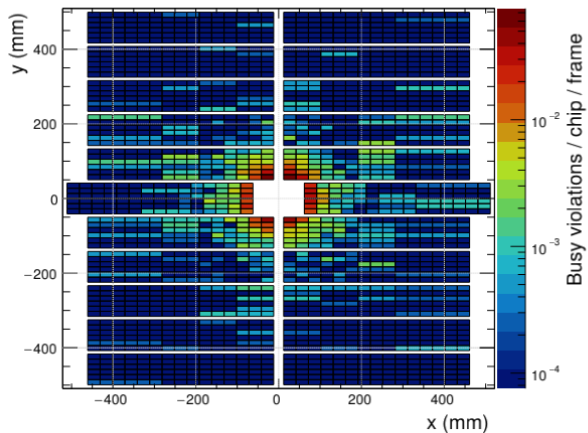There is no free slot in the MEB left to latch the pixel hits
The chip skips this trigger
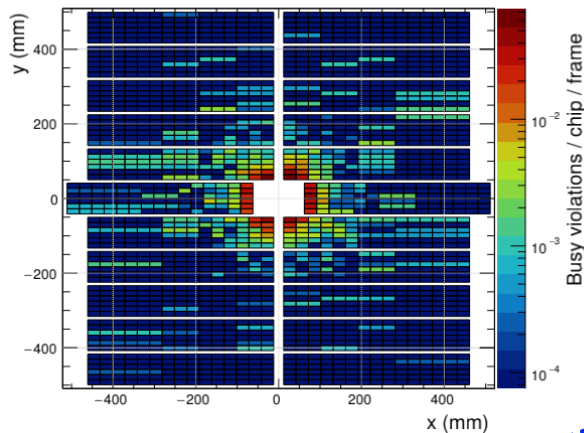The pixel hits are entirely lost for the newly requested time frame.

Occupancy event

Busy Violation

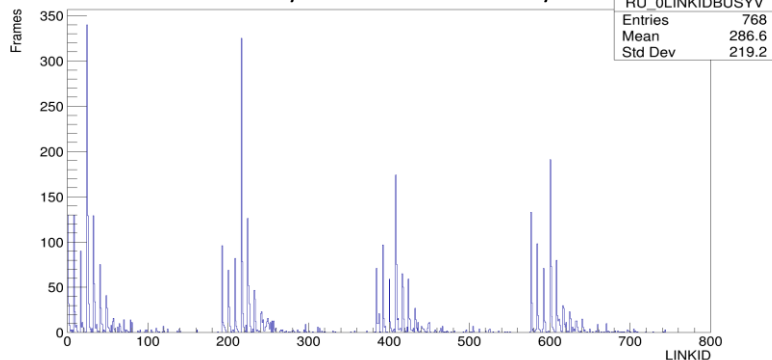FoCal Pixel Busy Violations Plane **5**

FoCal Pixel Busy Violations Plane **10**

Busy violation rate per chip:

$$r_{\mathrm{BUSYV}}(\mathrm{chip}) = \frac{N(\mathrm{frames\ with\ BUSY\ violation,\ chip})}{\mathrm{Number\ of\ readout\ frames}}$$
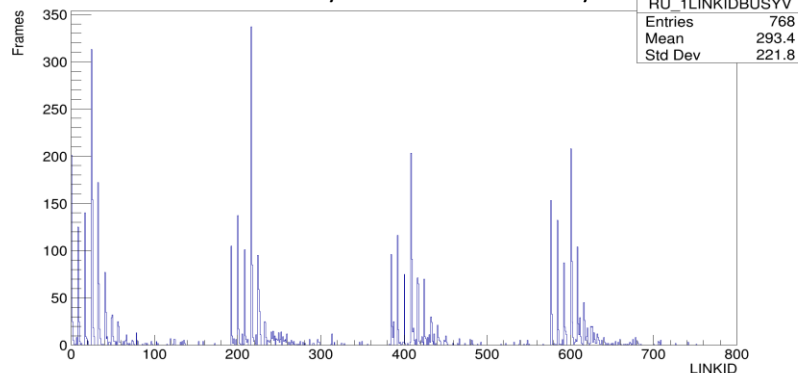
Busy violation rate per chip in the order of 5-6% in innermost chips

How long the BusyV duration would be??

Frames of Busy Violation each link layer 5

RU_0LINKIDBUSYV	
Entries	768
Mean	286.6
Std Dev	219.2

Frames of Busy Violation each link layer 10

RU_1LINKIDBUSYV	
Entries	768
Mean	293.4
Std Dev	221.8

The four links with the longest accumulated Busy Violation time are 24, 216, 408, and 600
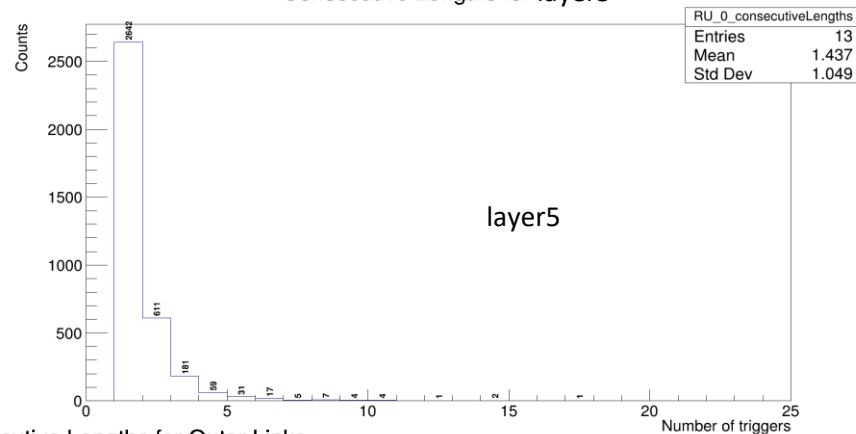
Jie Yi , 2023.11.17   12
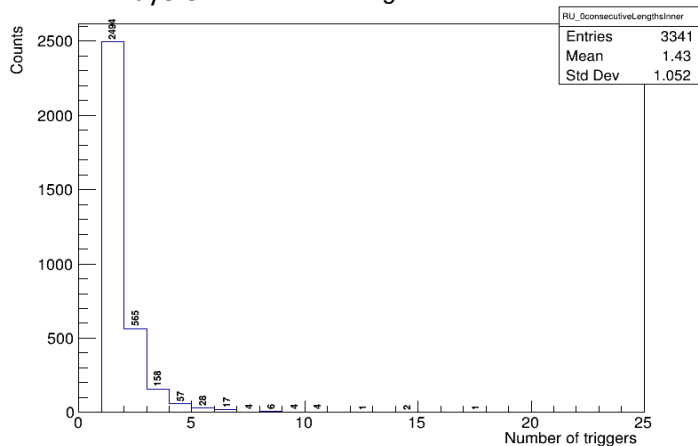
Layer 5:Duration of Busy Violation

Most are just single frame busy violation

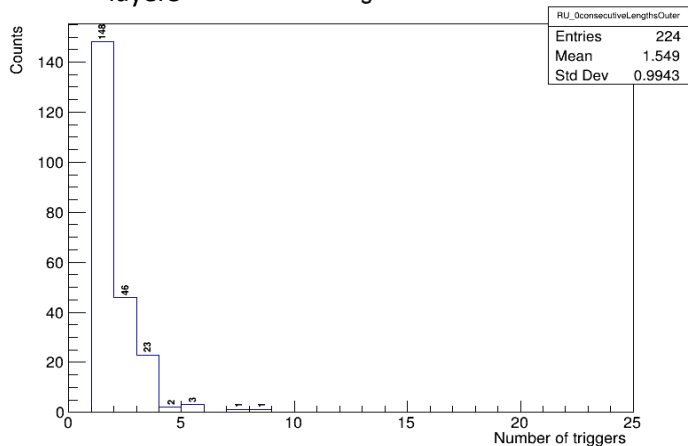Inner links are more susceptible to busy violation (tend to last longer)

Consecutive Lengths for layer5

layer5 Consecutive Lengths for Inner Links

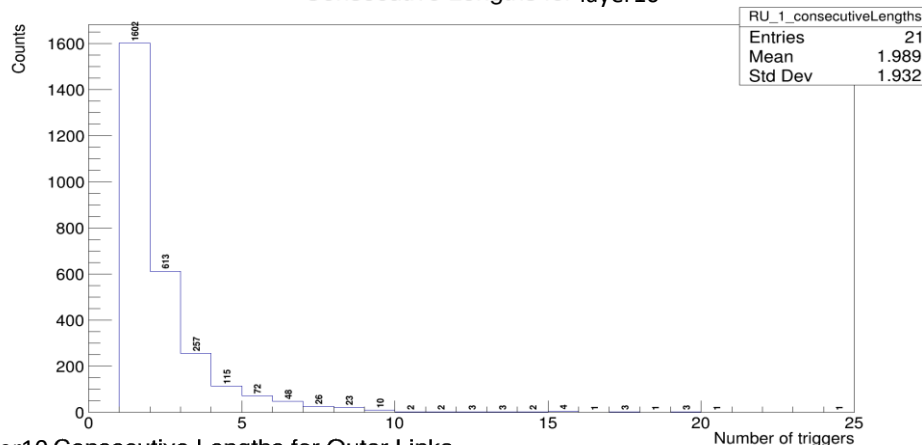layer5 Consecutive Lengths for Outer Links
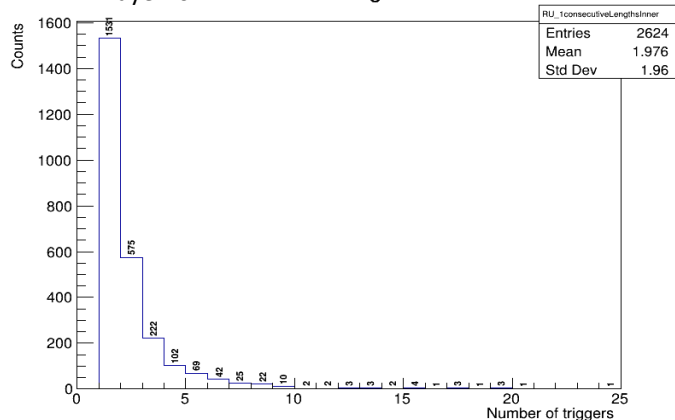
Layer 10:Duration of Busy Violation

Reduction in Busy Violations lasting just one frame

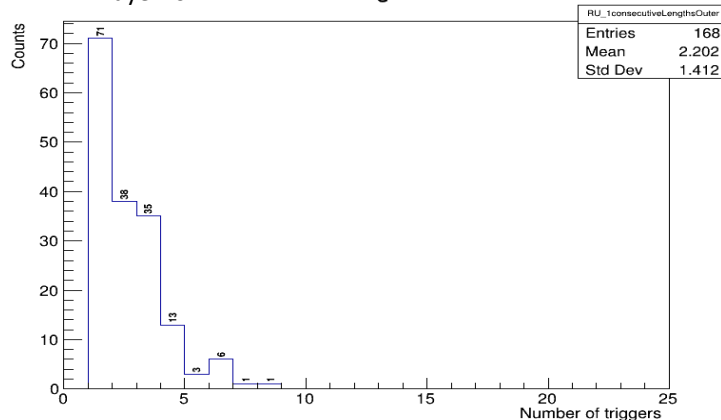Increase in longer durations of Busy Violation

Consecutive Lengths for layer10


layer10 Consecutive Lengths for Inner Links

layer10 Consecutive Lengths for Outer Links

Solution for Busy Violation

Various options are being studied:

- By back biasing the ALPIDEs, the average pixel cluster size can be reduced probably from 4 to 3, thus reducing the overall occupancy in the pixel by roughly a factor ¾

- Increasing the time frame length provides more time for the pixel matrix regions to be read out, and reduces the number of events which are being latched twice since less triggers are sent.
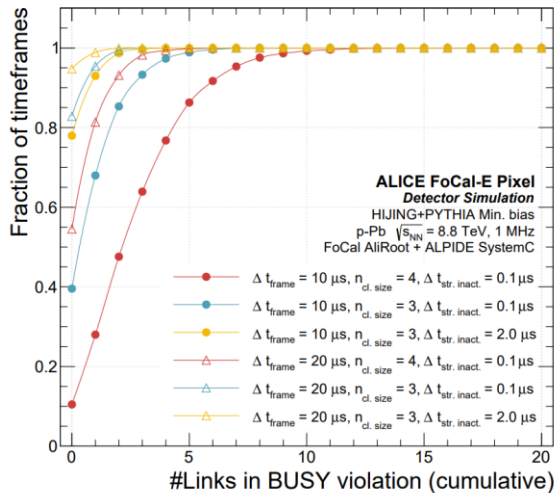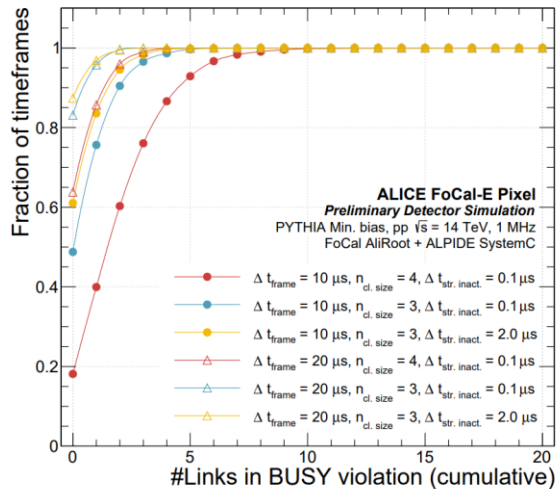
The fraction of frames which are not affected by BUSY violations is increased significantly by operating with a smaller mean cluster size (= 3) and an Δt inactive strobe of up to 2μs

Fraction of frames with the cumulative number of links in BUSY violation

Summary

- FoCal is part of the upgrade project of ALICE during Run 4 (starting from 2029)

- Link Saturation

-Inner link and outer link operate smoothly in most cases

-outer link have approximately a 1% probability of reaching link saturation

- Busy Violation

-Inner links are more susceptible to busy violation and they tend to last longer

-Most are just one single frame of Busy Violation

-Pixel Layer 1(Layer 10) tends to have a longer duration of Busy Violation

- Solution for the Busy Violation

Thanks for the attention!