# Irradiation test of ABCStar ASICs in CSNS

**Shaogang Peng**

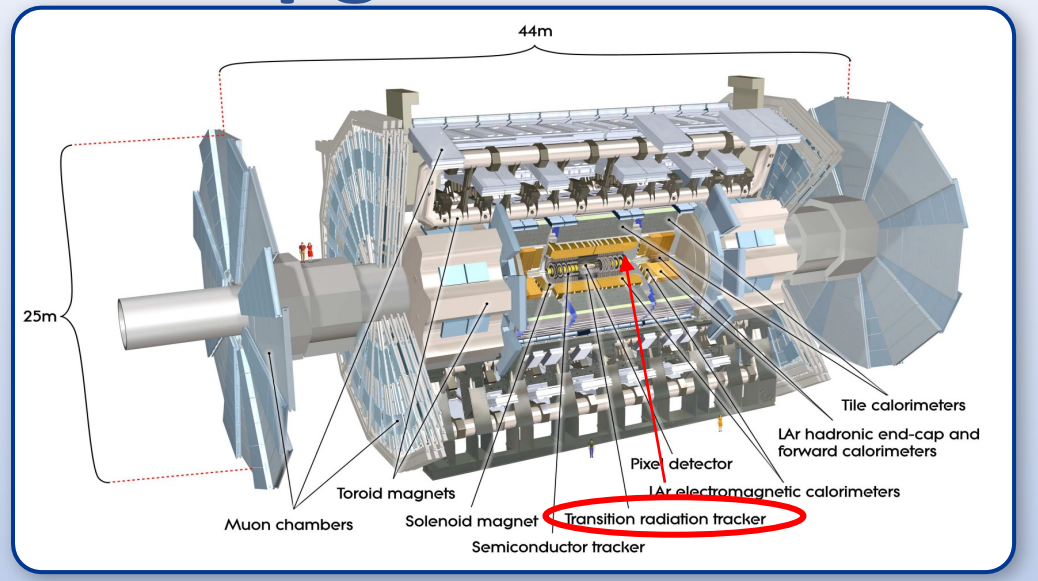
On behalf of ATLAS ITk Chinese group

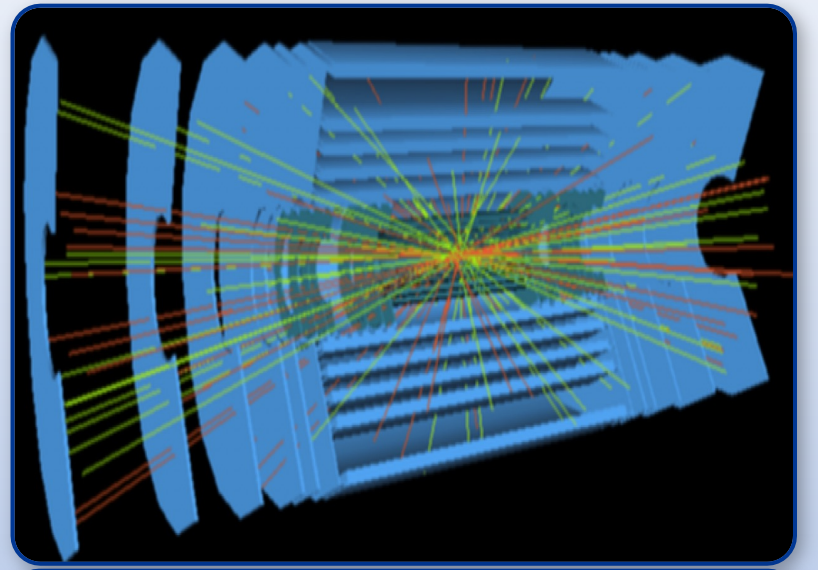
CLHCP 2023, Shanghai

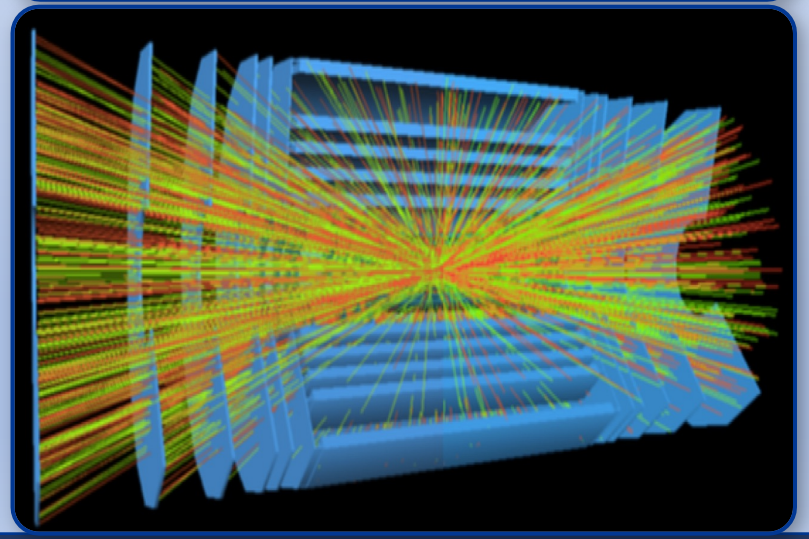
# Outline

- Introduction
- ABCStar V1 chip, SEEs and TID
- CSNS irradiation
- Results from proton tests
- Preliminary conclusion

# Phase II upgrade of ATLAS Inner Tracker for HL-LHC



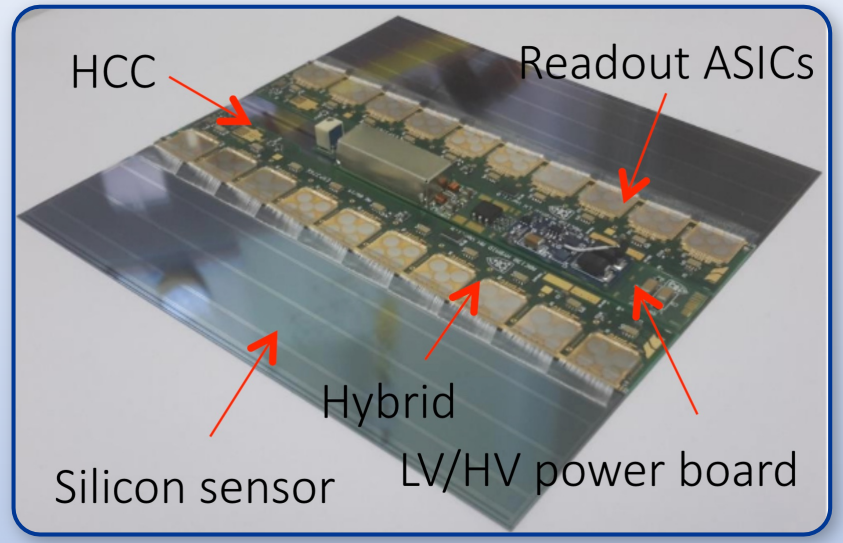



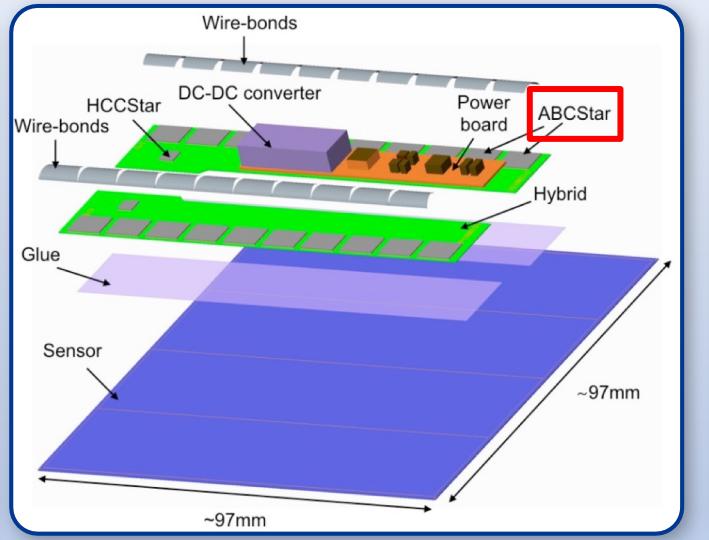


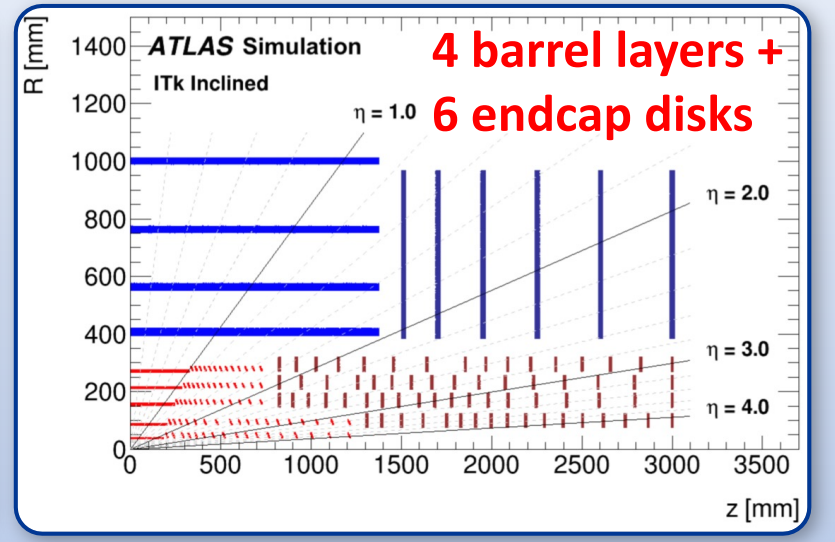
- All-silicon tracker will be built in the Phase II upgrade for the High Luminosity LHC (HL-LHC)
- The new detector will maintain or improve the **current ATLAS tracking performance (ITk)** to cope with the irradiation levels of the HL-LHC

# Inner Tracker (ITk)

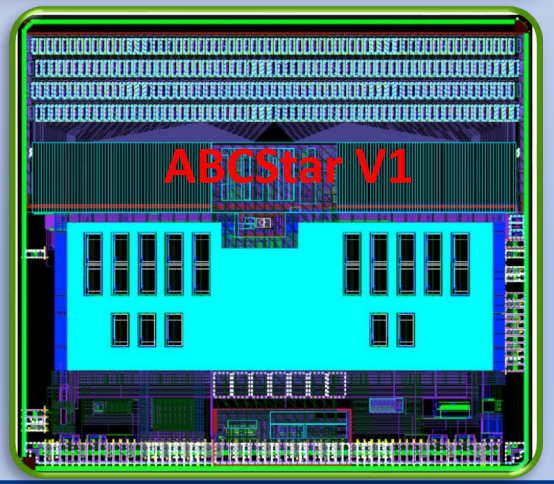
- **IHEP/THU contribute to the barrel of strip detector**



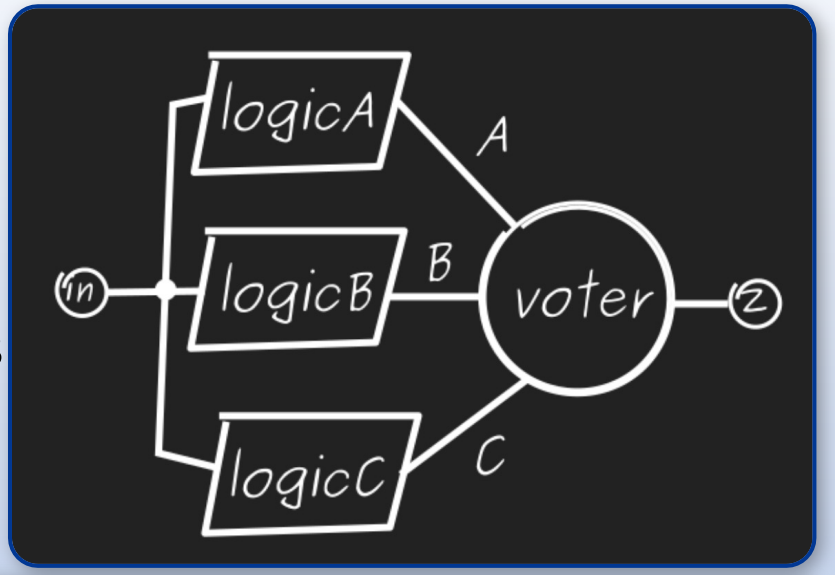




| Strip detector comparisons | Current Inner strip tracker (SCT) | Future ITK strip tracker |
|---|---|---|
| Radial distance | 300-560mm | 400-1000mm |
| Channels | ~8 millions | ~100 millions |
| Modules | 4 thousands | ~20 thousands (165m$^2$ silicon) |



# ABCStar V1 specification

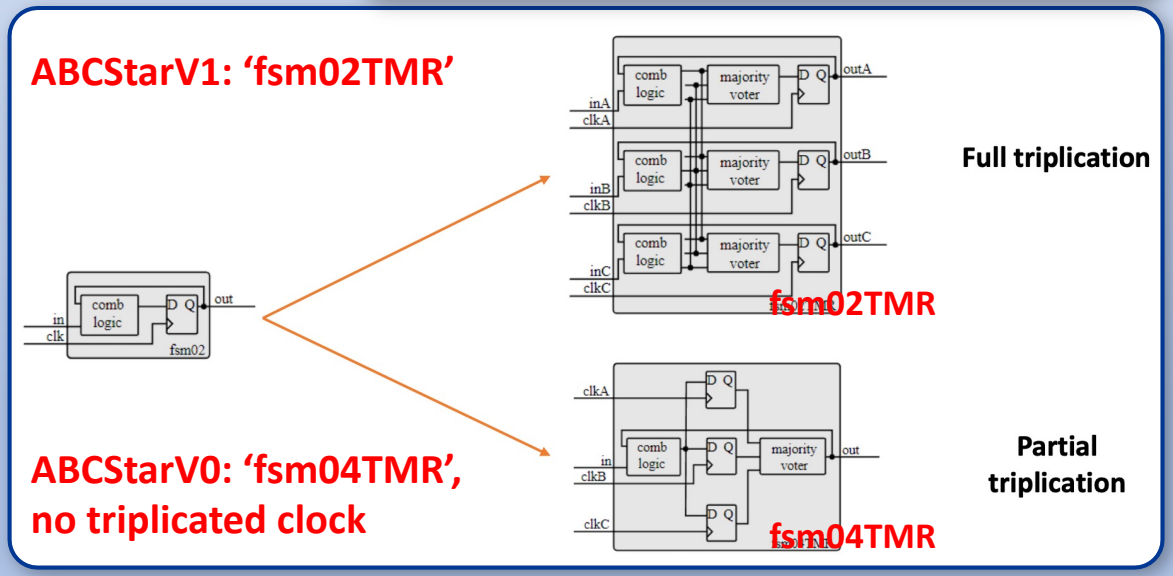
- 8 mm × 7 mm
- Fabricated using **130 nm CMOS** technology
- Read out signals from **256 sensor strips** by binary readout channels
- **Triple Modular Redundancy (TMR)**
  - Protect against SEEs




**TMR Variants**

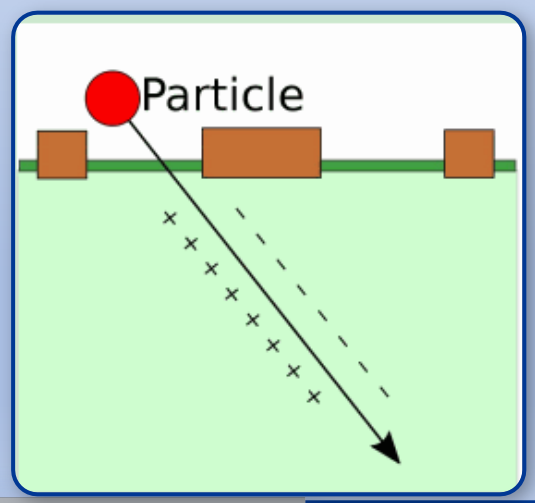
| | | Triplicated Registers | Triplicated Registers + clock skew | Full TMR |
|---|---|---|---|---|
| Resoures (power, area) | FF | x3 | x3 | x3 |
| | logic | x1 | x1 | x3 |
| | voters | x1 | x1 | x3 |
| | clocks | x1 | x3 | x3 |
| Speed | | +voter delay | +voter delay +clock skew | +voter delay |
| Protection | | ☹ | 😐 | ☺ |

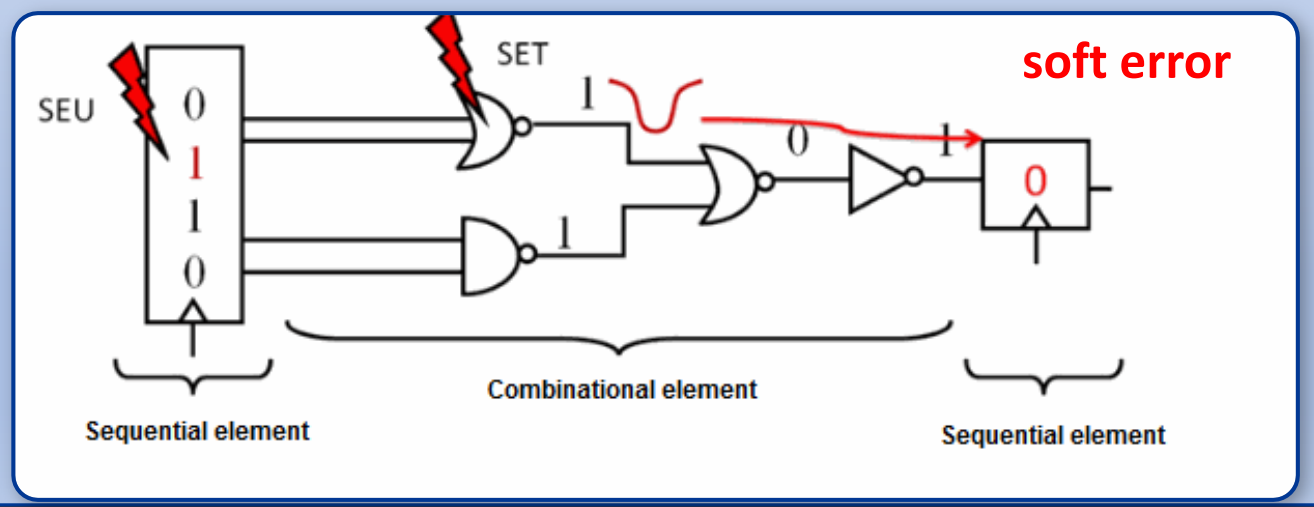
See here for more information about TMR



# SEEs

- Single Event Effects (SEEs) – electrical disturbance of an electronic device interacts with high-energy particle
  - **Single Event Upset (SEU)** – affects both dynamic and static memory registers storing logic states by collecting charge → **voltage change** → bit flips happen
  - **Single Event Transient (SET)** – a transient pulse produced by a charged particle in a circuit → **temporal disorder** → bit flips happen



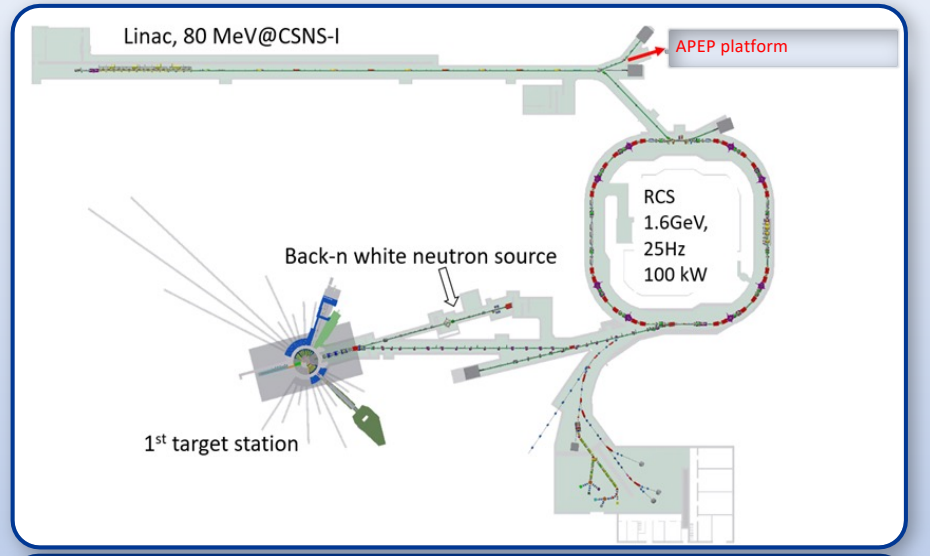



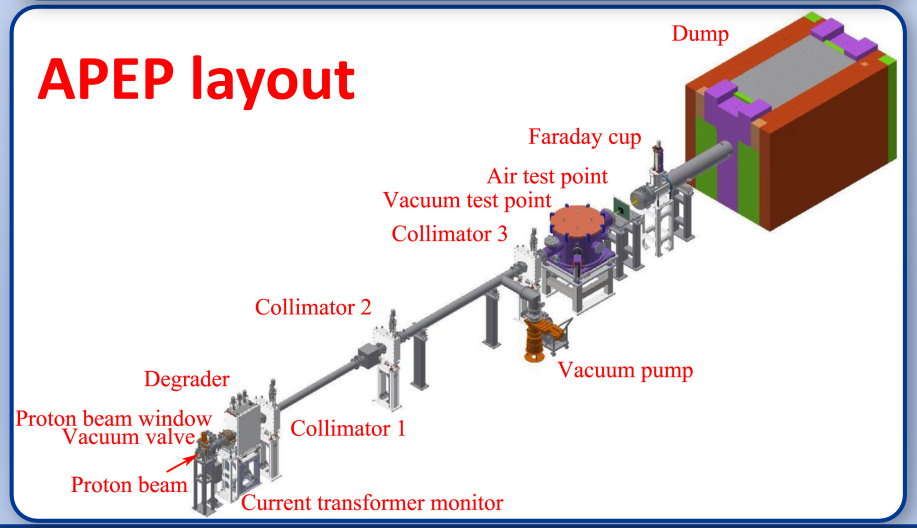
# Total Ionzing Dose (TID)

- An **increase in digit current** when chips exposed to ionizing doses of radiation
- Up to **approximately 1 Mrad**
- Continued exposure gradually reduces the current back towards **normal value**
- Refers to the cumulative amount of radiation
- The sensitivity of microelectronics to TID can impact reliability and functionality

# Proton beam at China Spallation Neutron Source (CSNS)

- We utilize the **Associated Proton Experimental Platform (APEP platform)** to have irradiation on ABCStar chips at the end of the CSNS linac
- To validate the performance of ABCStar ASICs V1 and V0, irradiated **2 campaigns:**
  - May 2022: 80MeV, **one V0 chip**
  - April 2023: 20MeV ~ 80MeV, **four V1 chips**
- Beam spot → **20mm × 20mm**
- Flux: $1.16 \times 10^7 \rightarrow 2.66 \times 10^9$ p/cm$^2$/s
- Fluence: $1.24 \times 10^{14} \rightarrow 3.63 \times 10^{14}$ p/cm$^2$
- Dose: ~ 40 Mrad
- **~ 170 hours** totally



# ABCStar beam test

- ABCStar V1 chips under the same energy undergo different running scenarios
  - **Clock disable**(disabling one of the triplicated clocks)
  - **Glitch Filter**(delay incoming signal 1.3 ns)
  - **BCID**(one mode of filling the ABCStar's event data)
    - **More realistic approximation of real event data**
  - **Idle**(repeating binary data "0110" instead of "0000")
  - **Latency 20/503**(the data is stored in the ABCStar buffer for a period of time)
- Why we set diffent energy to have irradiation?
  - **Linear Energy Transfer (LET)** is not same at different energies

# Cross section (XS) of SEU

$$\sigma_{SEU} = \frac{n_{0\to1} + n_{1\to0}}{\int d\phi}$$

$n_{0\to1}$ and $n_{1\to0}$ are the number of $0 \to 1$ and $1 \to 0$ bit flips

The cross section is normalized to the total integrated fluence

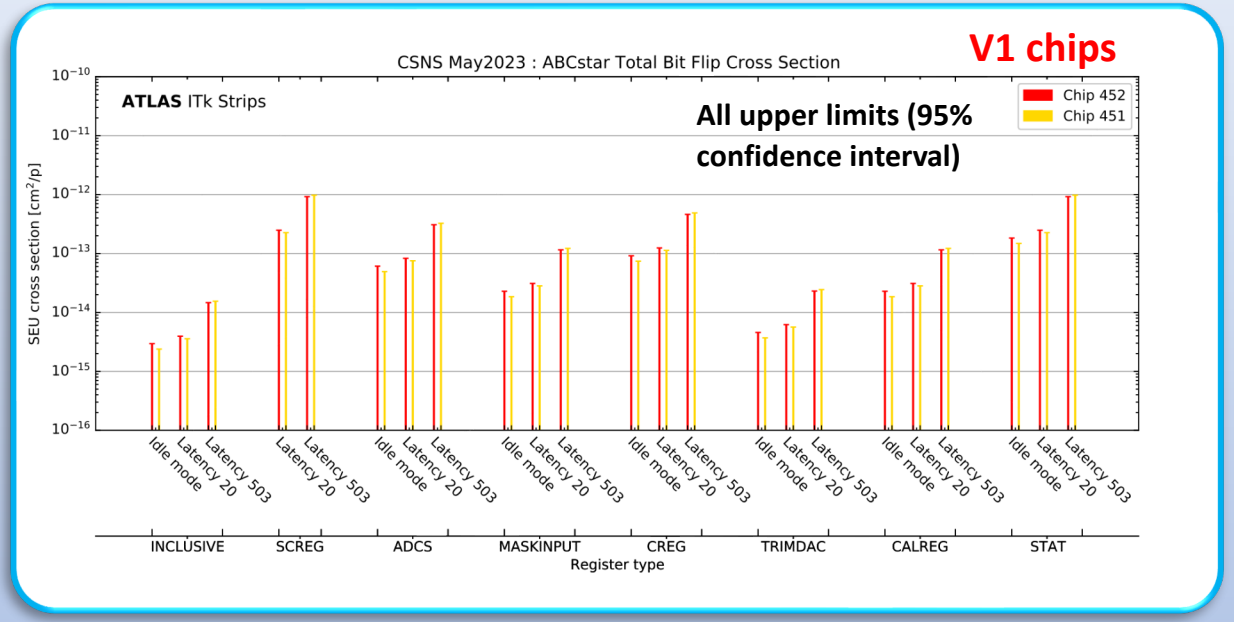
$$\Delta\sigma_{SEU} = 1.96 \times \frac{\sqrt{n_{0\to1} + n_{1\to0}}}{\int d\phi}$$

In the case of zero measured SEUs, 95% upper confidence bound is calculated

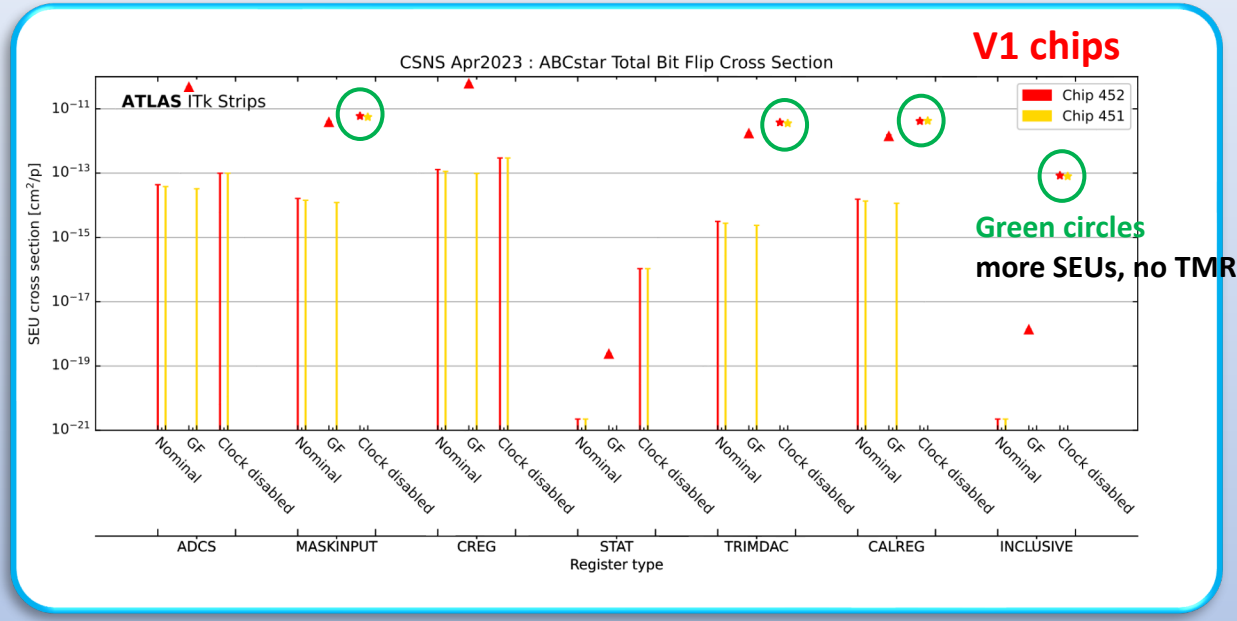
**by assuming 3 SEUs**

**(Poisson statistics distribution)**

# SEE XS of registers with different modes



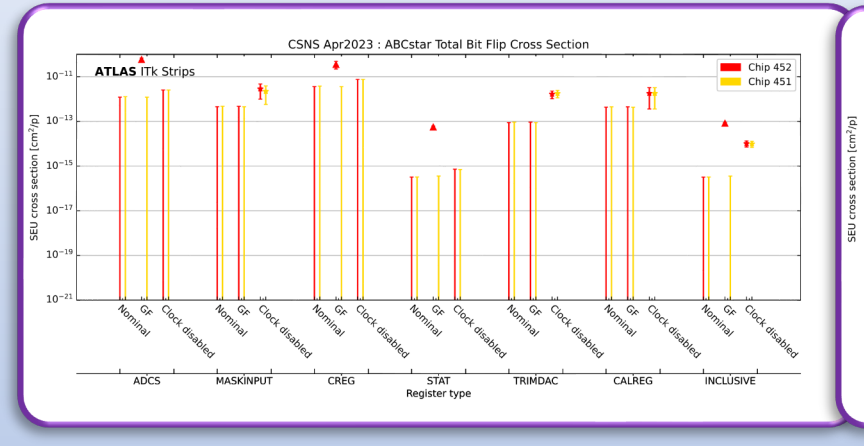

80 MeV



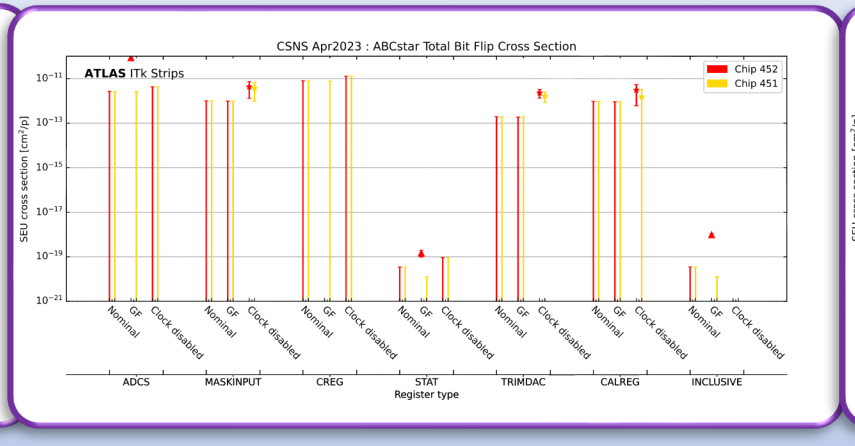

80 MeV

- **If the cross section dependence on the data latency in buffer? No**
- TMRs do enhance the irradiation hardness of ABCStar chips to SEE

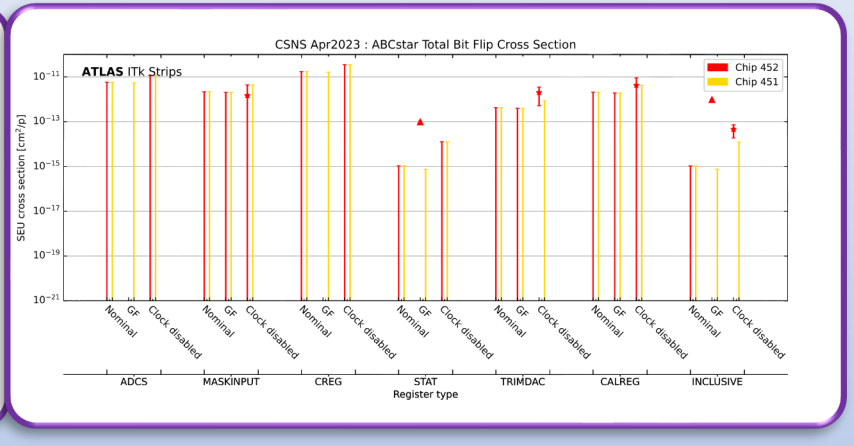
# SEE XS of registers at different energies




60 MeV




40 MeV



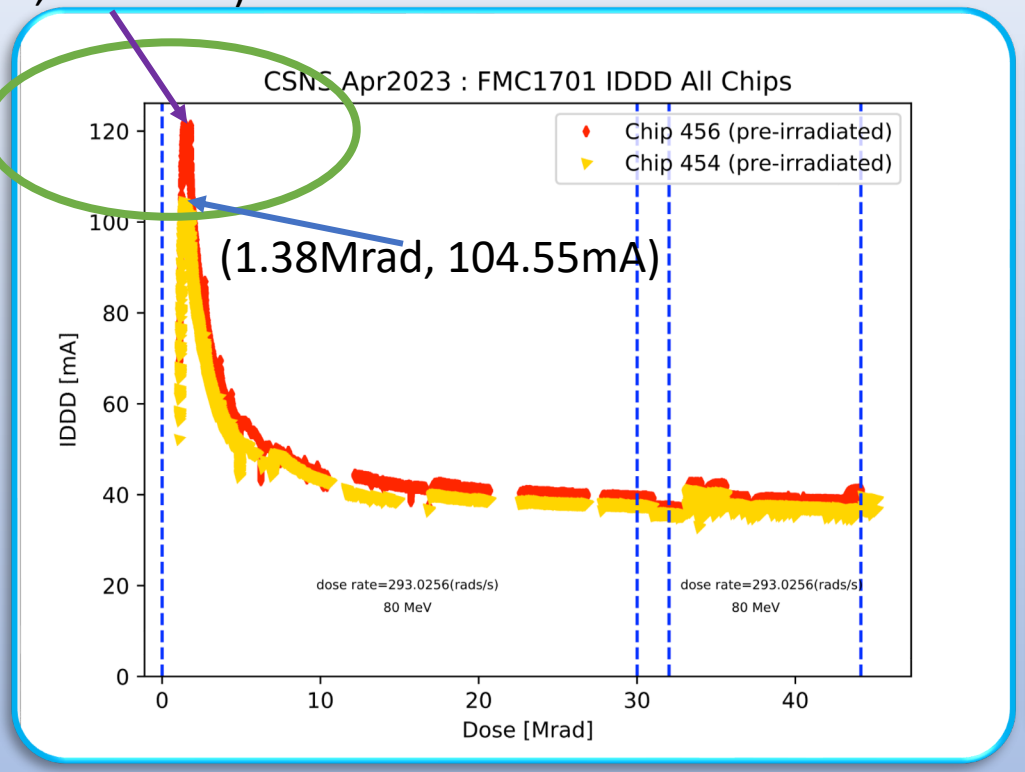

20 MeV

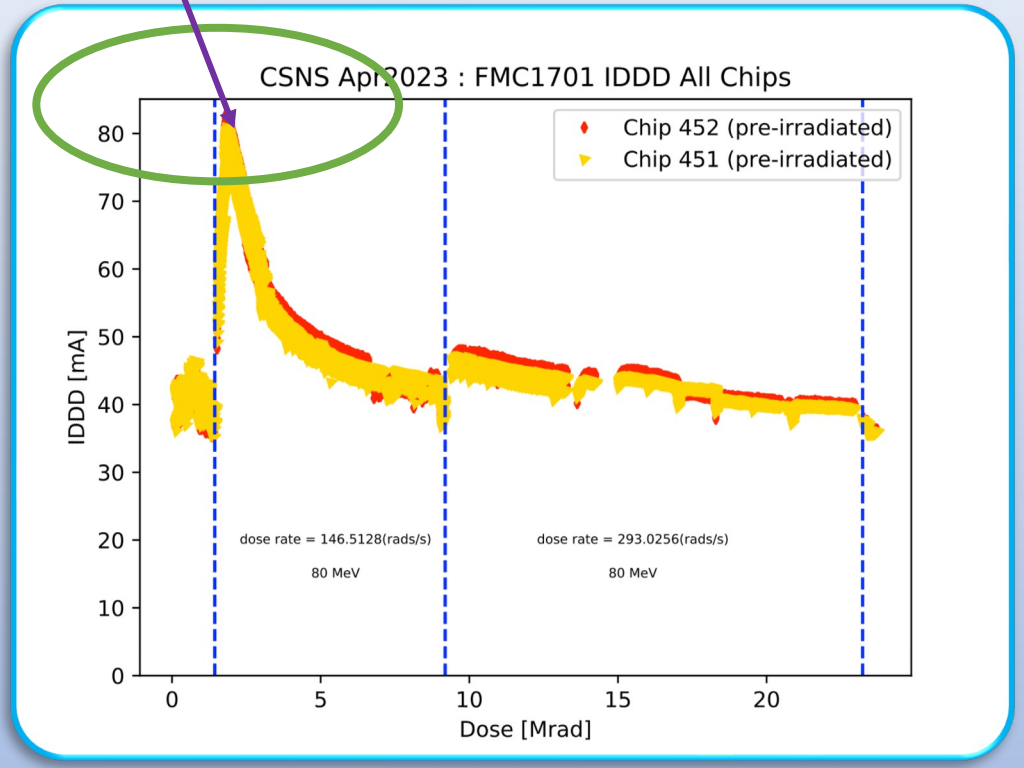
- **Bit flips still happen with a certain probability when lower energy (20MeV)**
- **LET result in variations of the XS at different energies**
- **XS does not exhibit a clear pattern of variation with energy for the same register under the same mode**

# TID results

(1.40Mrad, 121.7mA)

(1.8Mrad, 80mA)




- Different dose rate is utilized at the same energy
- TID bump appears **at around 1 Mrad** as expected and pertains to the irradiation history

# Preliminary conclusion

- SEE irradiation test about ABCStars have been performed at the APEP in CSNS.
- ABCStar V1 in which more TMR are implemented are more radiation hard as expected.
  - Register, logic of data transition, clocks
- The analysis of SEE cross section in physics packets is ongoing

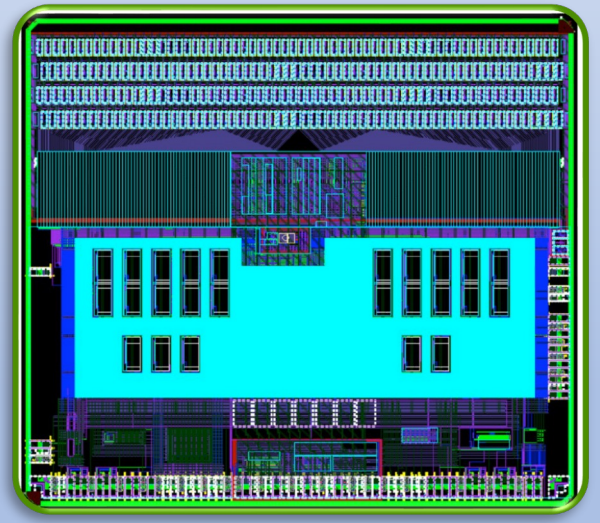
# Thank you!

# backup

- The binary outputs produced by each front-end channel are captured and retained in the chip's Level 0 Buffer(L0_Buffer)
- The ABCStar architecture supports a multi-trigger data flow
  - **L0 trigger (L0A, with L0tag added):** event data from the **beam crossing synchronous pipeline (L0Buffer)** is copied to the EventBuffer memory
  - **LP (Low Priority) trigger**: a first asynchronous readout request with priority and low latency for fast processing of track information
  - **PR (Priority Request) trigger**: A second **asynchronous readout request** intended for a global readout

# ABCStar V1(compared to V0) new modes

- **SEU counter (8-bit)**
  - Increases when a SEU is encountered in the registers: ADCS0, ADCS1, ADCS2, CREG0, CREG1
  - Not indicate register errors, but the occurrence of an upset and a subsequent corrective action
- Clock disabling
  - Disabling one of the triplicated clocks effectively increases the cross-section **by a factor of 2**
- Glitch filter
  - Delay a copy of the incoming signal **by 1.3 ns** and compares the copy with the original
  - The signal is not propagated further if they do not match
- Idle pattern
  - Programmable pattern **(repeating "0110", default "0000")**
- Latency setting(Latency 20/503, more SEUs)
  - Data is stored for some period of time awaiting a trigger
- Programmable multiplexer
  - Allows external output pin ("TESTOUT") to reflect internal signals inside ASICs
- Packet structure
  - **68 bits**
  - Difference exists between V1 and V0, see here



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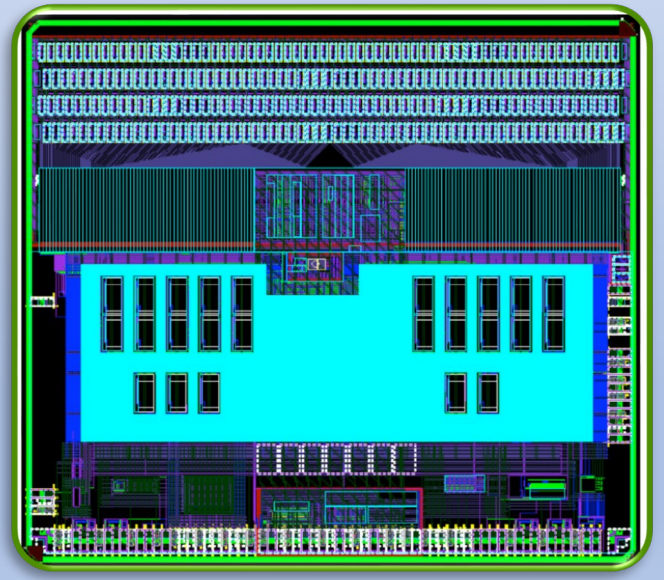
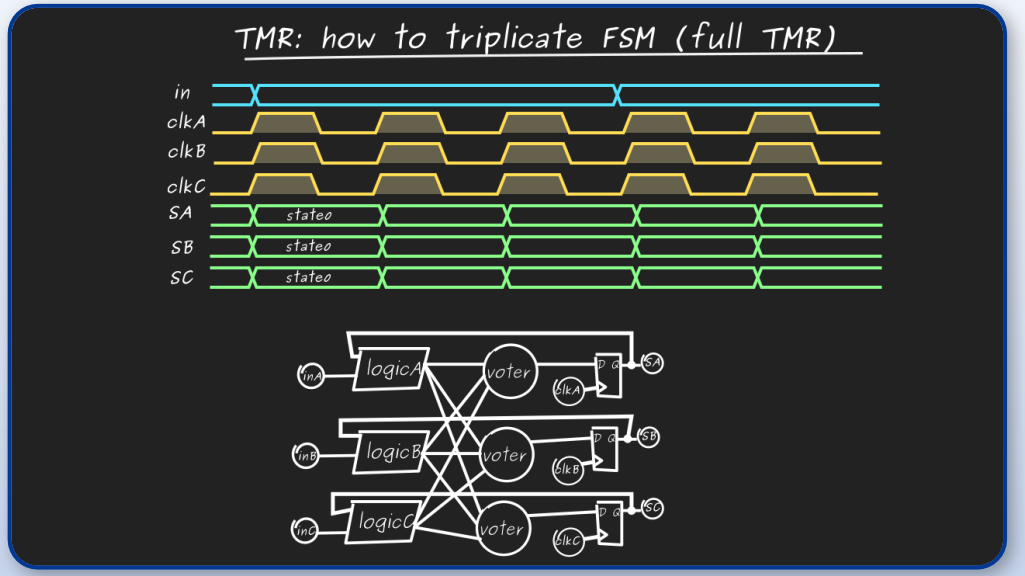
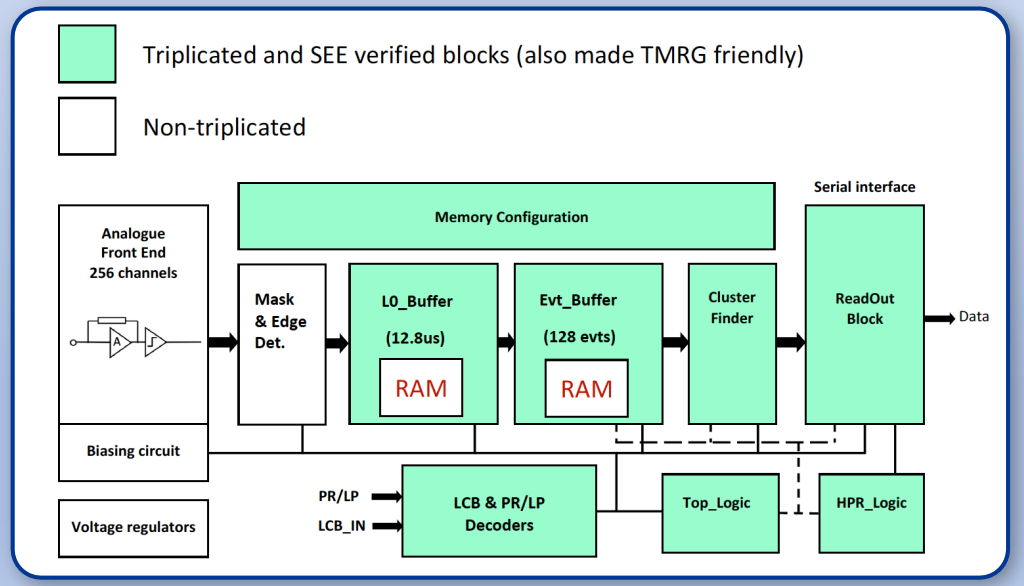
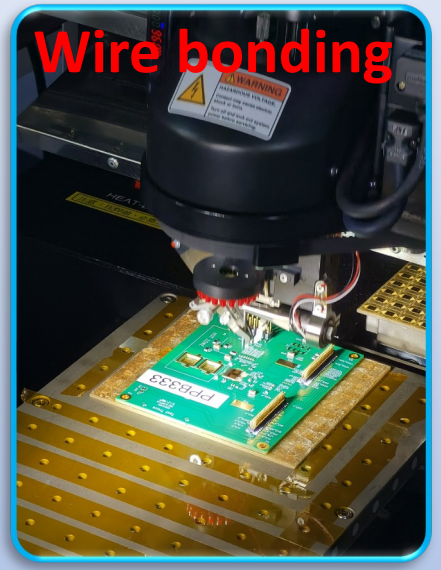
- Designed to read out signals from **256 sensor strips** through binary readout channels
- Triple Modular Redundancy (TMR)





# ABCStar beam test


# Cross-section (XS) of SEE

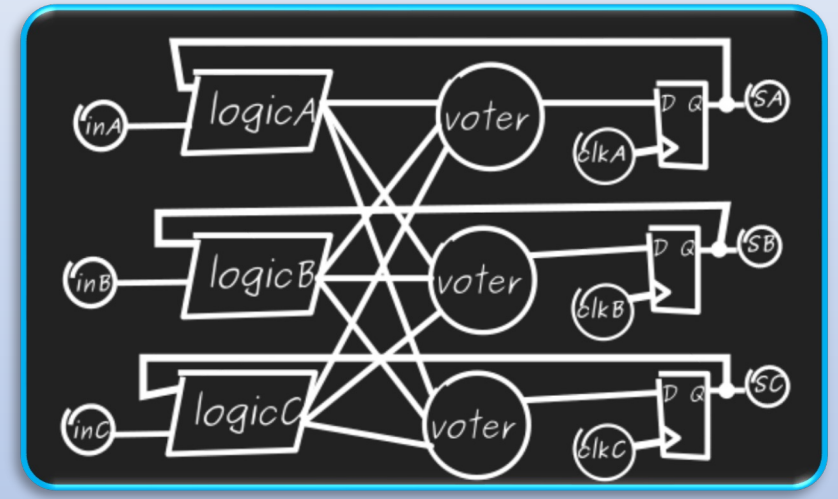
**XS = (total number of occurences) / (total integrated fluence)**

- For a nonzero number of occurences, a **95% confidence interval** can be determined as follows:

$$\sigma(\mathrm{XS}) = 1.96 \times \sqrt{(\text{total number of occurences})} / (\text{total integrated fluence})$$

# Register read XS

- Registers store configuration and counters
  - **V1 chips have fully triple modular redundancy (TMR) (mitigate SEUs)**
  - **V0 chips don't have fully TMR**
- Bit flips can be counted by comparing the expected register bits with the measured during repeatly readout




More information about TMR see here, the image is from *Stefan Biereigel and Szymon Kuli*