Simulation of UT for LHCb Upgrade II

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on behalf of the LHCb collaboration

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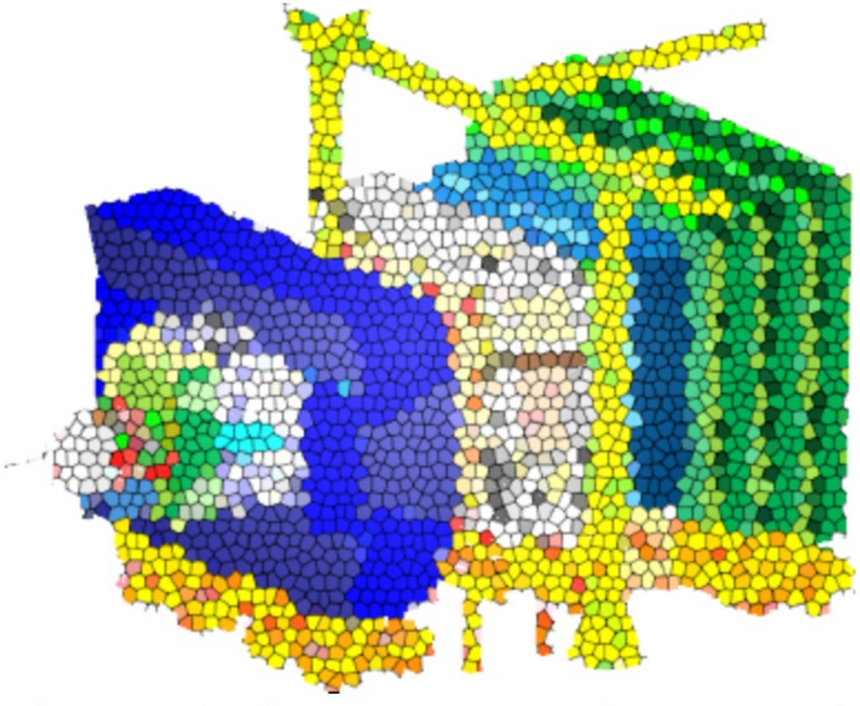
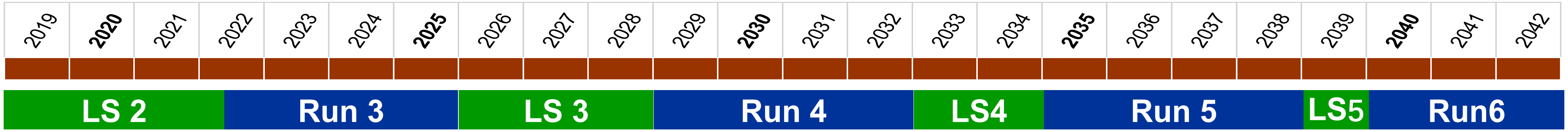
Outline

1. LHCb Upgrade II Introduction
2. Simulation progress of UT detector
    2.1 Fake digitization
    2.2 Full simulation and reconstruction
    2.3 Physics performance studies

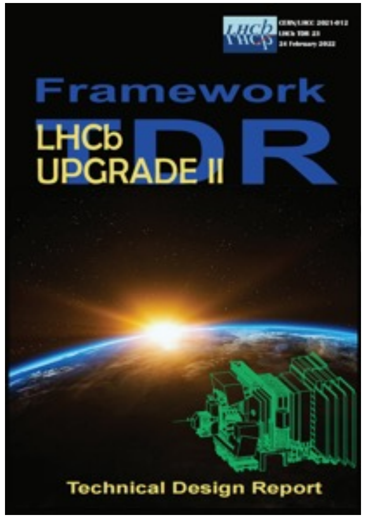


LHCb Upgrade II



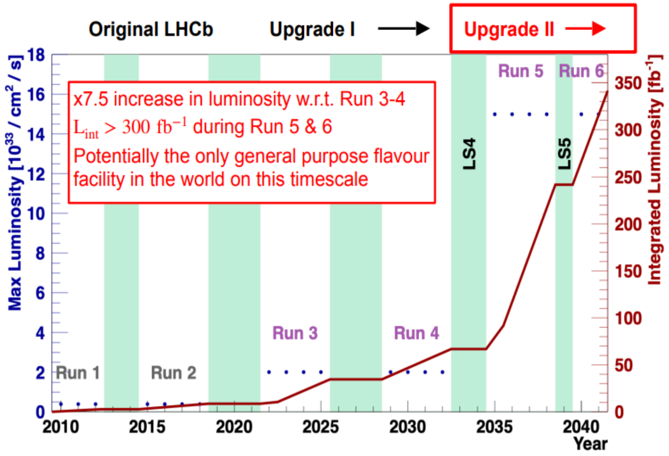
Upgrade II Installation

- FTDR was approved in March 2022
  - Detector design and technology options
  - R&D program and schedule
- Scoping document
  - Need to complement with more detailed plans on the scoping options and with analysis of physics performance
  - Target is to produce the doc within 2024
- Upstream tracker (UT) for Upgrade II
  - Use Upstream Pixel (UP) to replace the name U2UT
  - Many progresses have been made in simulation and software



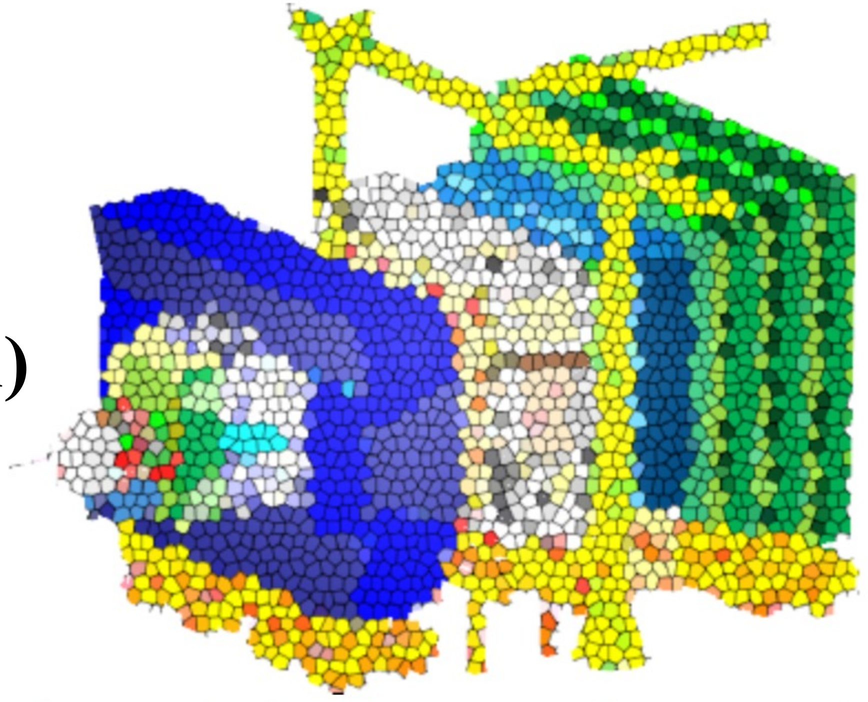
CERN/LHCC 2021-012; LHCb TDR 23

$\mathcal{L} = 1.5 \times 10^{34} cm^{-2} s^{-1}$



Upgrade II timeline

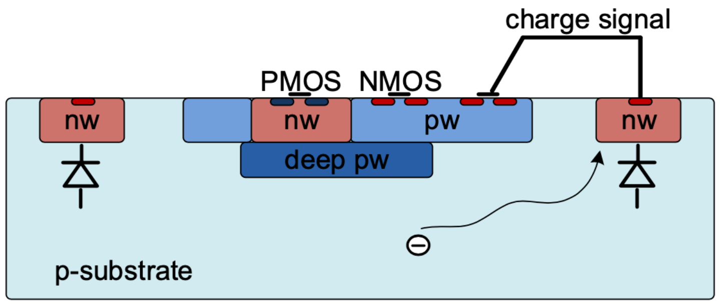
1. LHCb Upgrade II Introduction
2. Simulation progress of UT detector
    2.1 **Fake digitization (Fast simulation)**
    2.2 Full simulation and reconstruction
    2.3 Physics performance studies



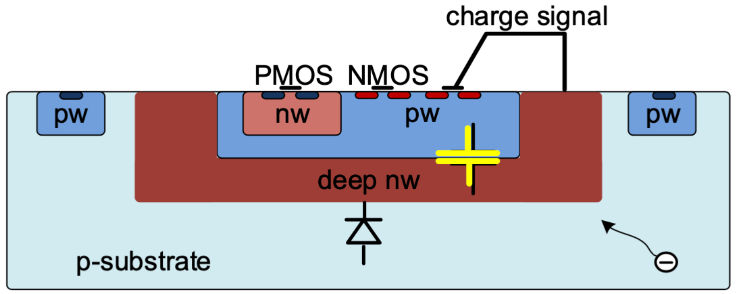
CMOS Sensor Options

- The ongoing R&D studies indicate that monolithic active pixel sensors (MAPS) can be considered as very strong candidates for Upgrade II UT.
- Following two different approaches, namely large fill-factor or high-voltage (HVCMOS) and low fill-factor or low-voltage (LVCMOS) with small electrode.

Characteristics	LV-CMOS	HV-CMOS
Chip size	3.5×3.5 cm^2	2.0×2.0 cm^2
Pixel size	30×30 um^2	50×150 um^2
Chip thickness	~ 100 um	
Position resolution	5-10 um	15, 40 um
Time resolution	O (1) ns	
Power consumption	100 – 300 mW/cm^2	
Radiation dose	3×10^{15} n_{eq}/cm^2, or 240 MRad TID	
Data rate per chip	Up to 30 Gb/s	Up to 9 Gb/s



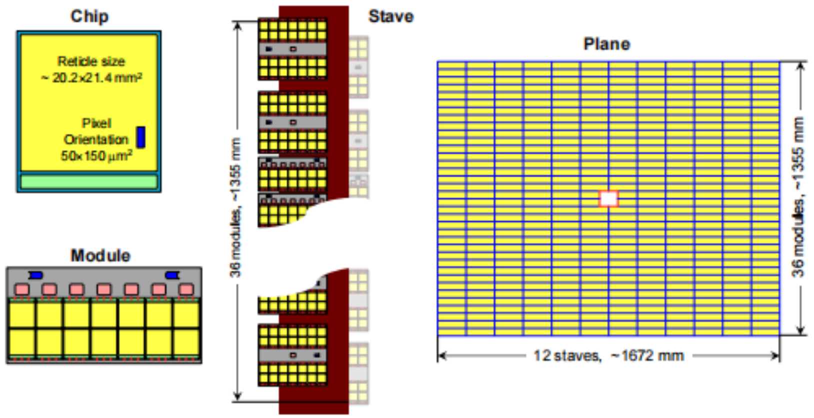
CMOS with small electrode

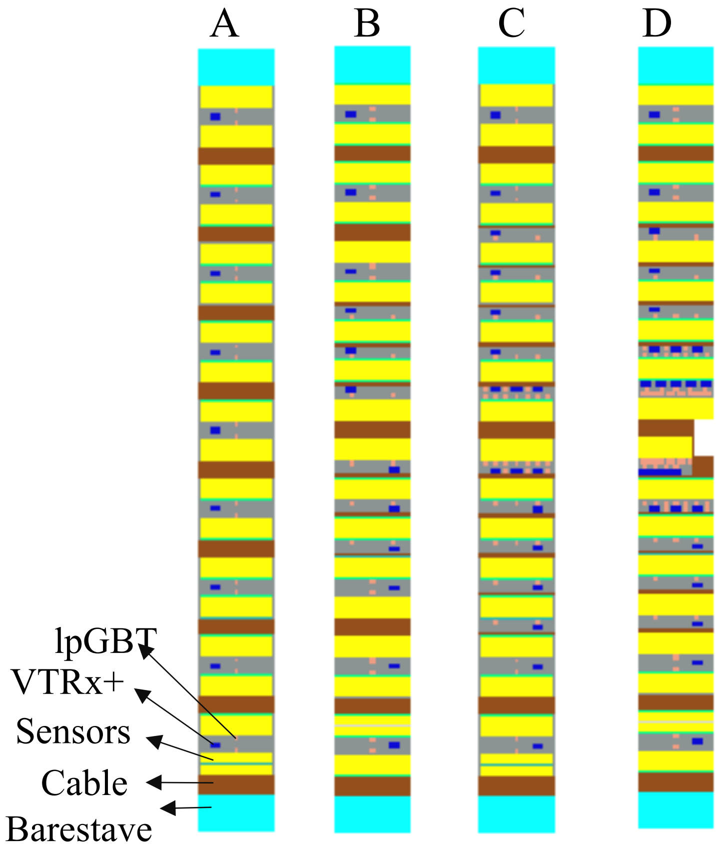


High Voltage CMOS

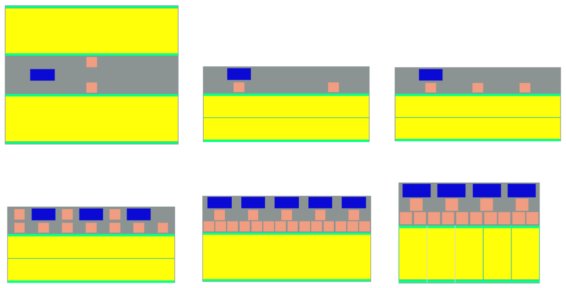
UT for Upgrade 2

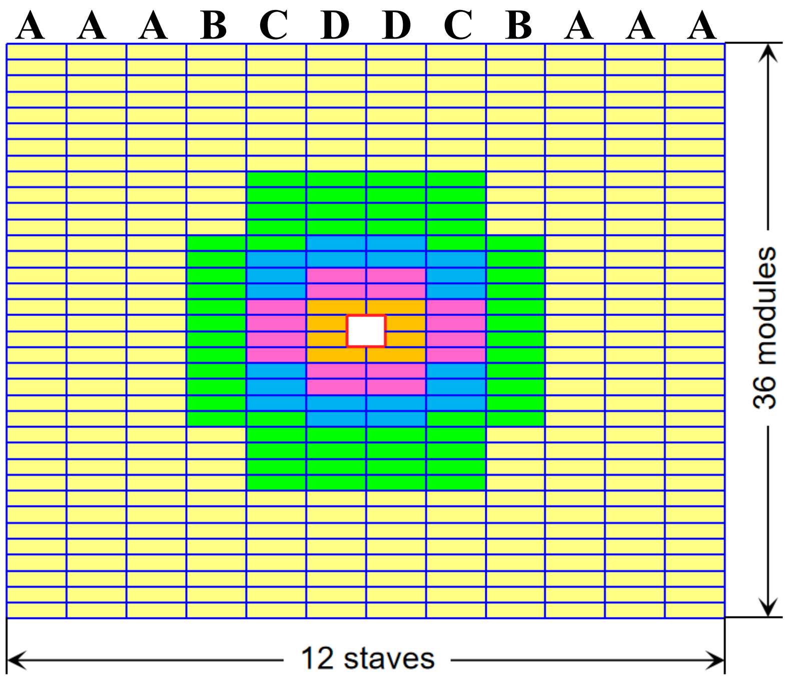
- A design based on HV-CMOS MAPS tech.
  - Described in FTDR
  - Can be adapted for CMOS with small electrode
- "Fake digitization" study based on MCTruth level
  - Geometry @ Gauss/Gaussino level





Ring	5	4	3	2	1	All
e-links / chip	1	1	1	1-3	2-7	
Gbps / e-link	0.32	0.64	1.28	1.28	1.28	
lpGBT / module	0.5	1	2	7	14/10	
Num of modules	1312	240	80	64	32	1728
Num of data lpGBTs	656	240	160	448	384	1888
Num of ctrl lpGBTs	656	240	80	192	144	1312

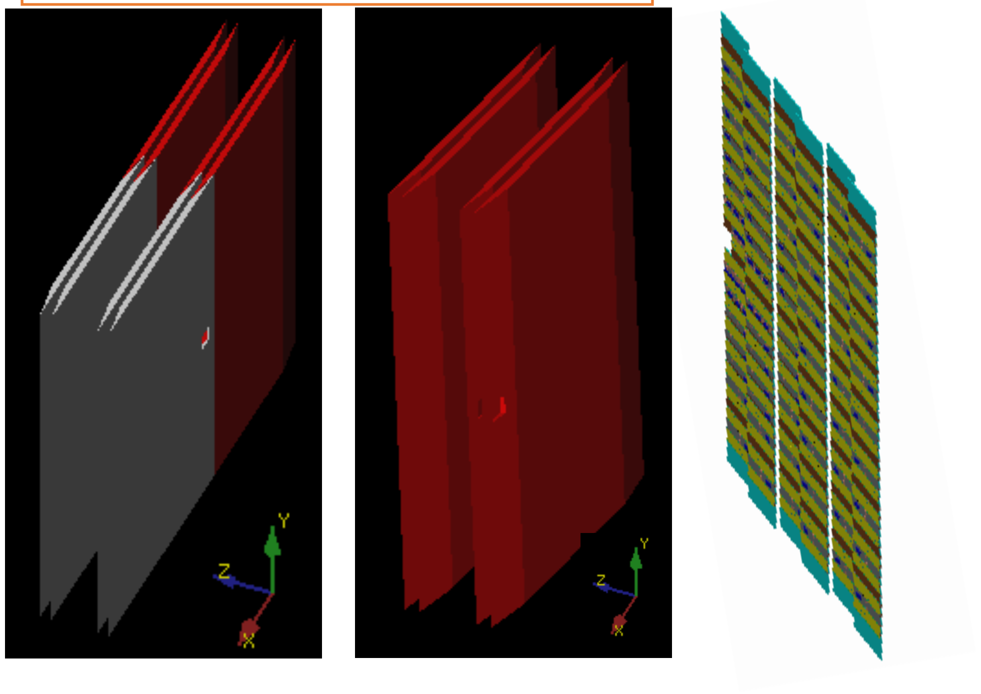

6 types of module



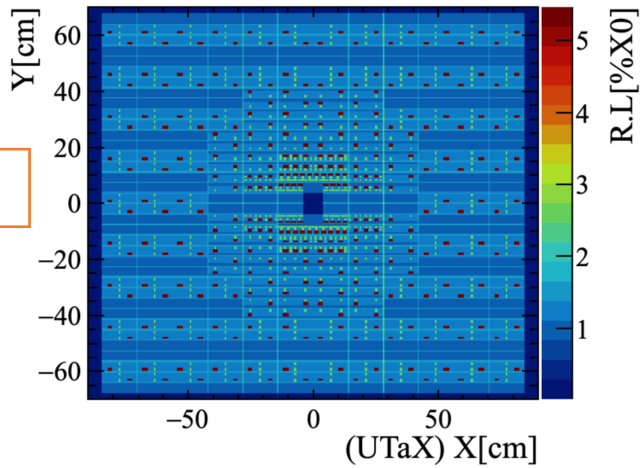
Detector Geometry

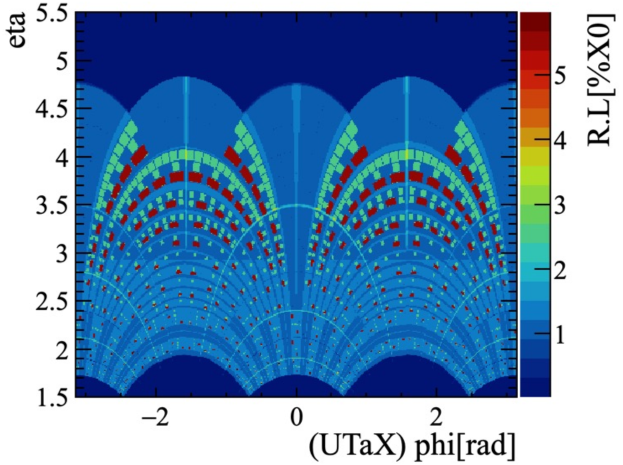
- DD4hep is widely used to replace DetDesc
- Detector modelled in DetDesc & DD4hep
  - Coding started in DetDesc, porting into DD4hep
- Material budget studied
  - Both in DetDesc & DD4hep frameworks
- Detector modelling implementation
  - Gauss jobs in both frameworks all good
- Working on merging the geometry in DD4hep to match the recent released $Detector project

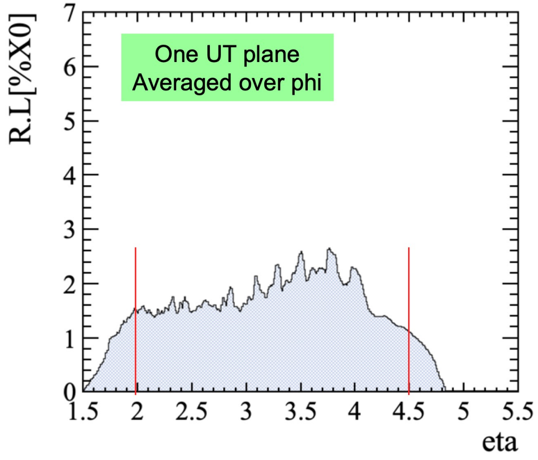
UP detector by Panaramix



R.L. in DD4hep







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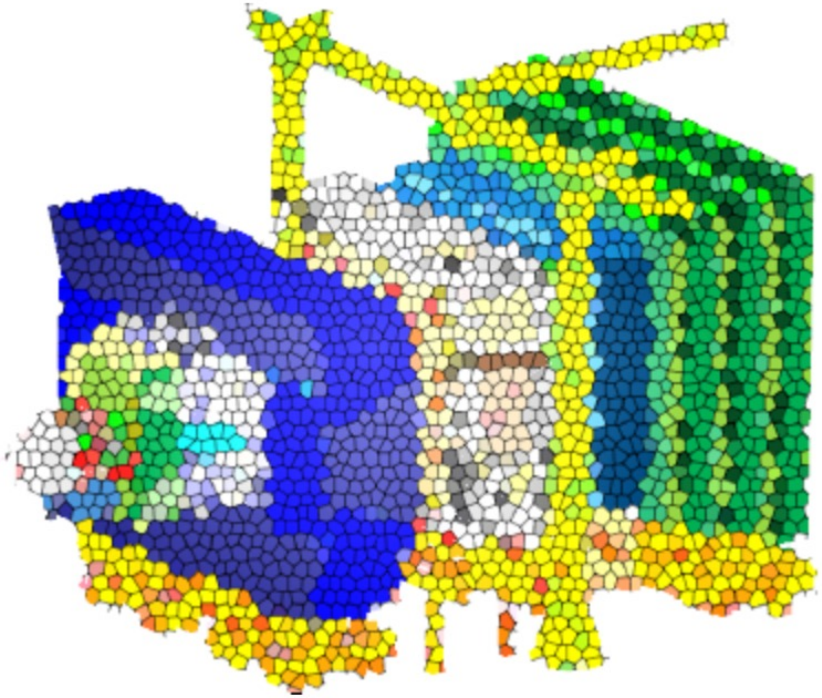
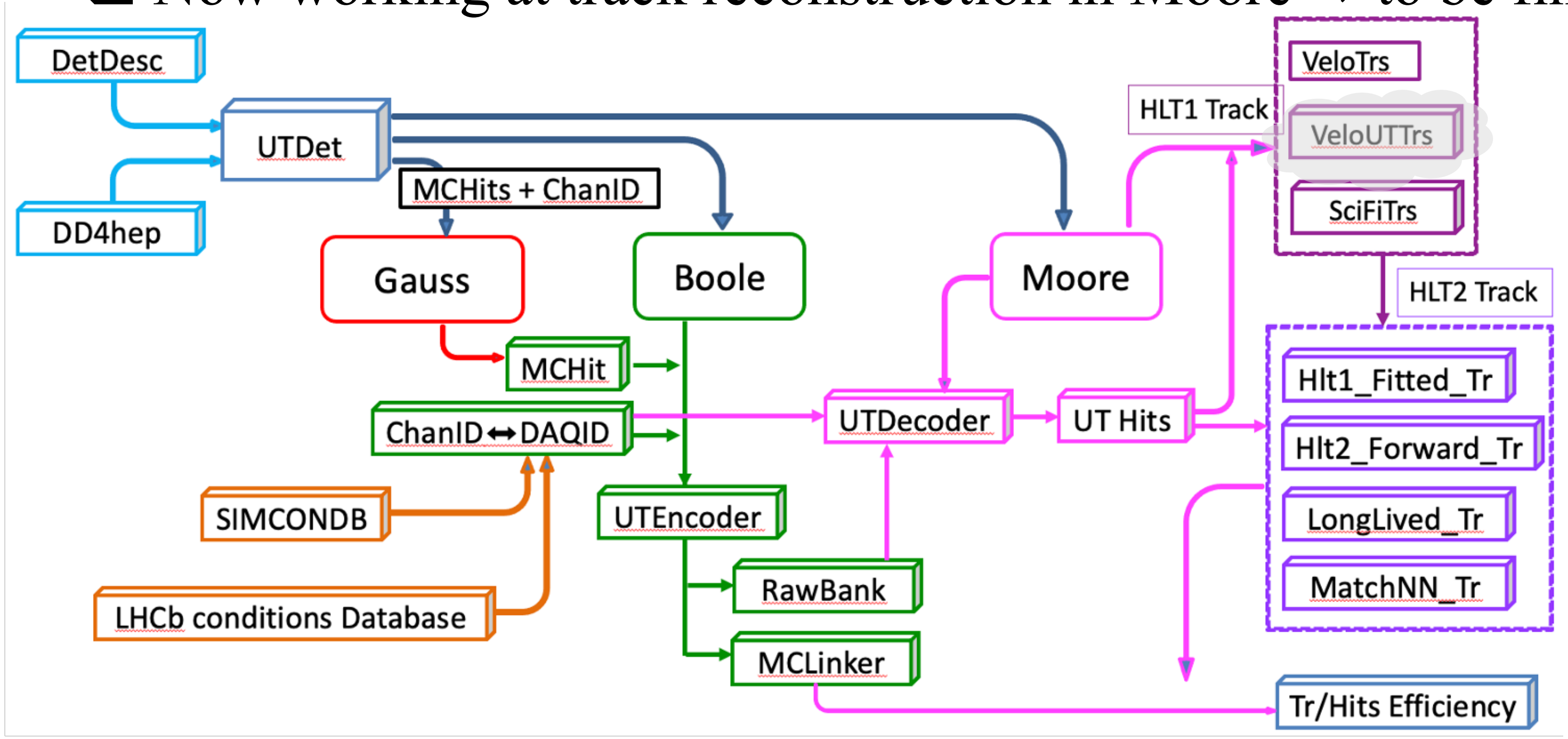


Full simulation for UP

Current UT software as a template but pixel sensors replacing old strip ones

- In DetDesc framework, Detector interaction (Gauss) and digitization (Boole) have been implemented.
  - Now working at track reconstruction in Moore ⇒ to be finished by this winter



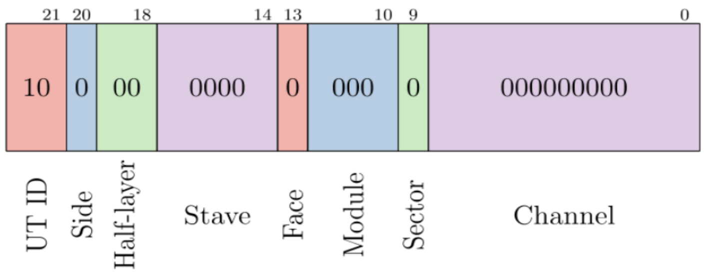
- ChanID, DAQmap, RawBank en/decoder designed for UP
- Magnet Station (MS) added in Tracking system
- Working on VeloUT track reconstruction

New UP Channel ID

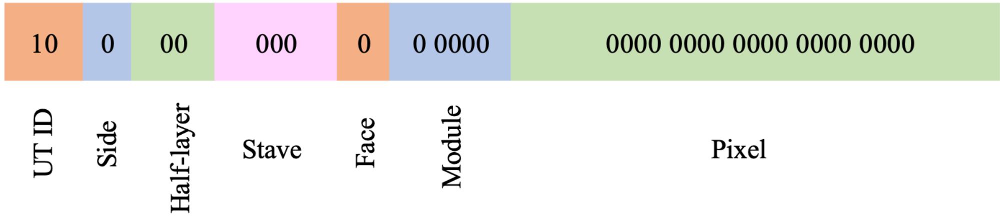
New IDs for UP

- ➢ Each pixel has one unique ID (ChannelID)
- ➢ Software updated using new UTChannelID
  - Labelling hits in detector
  - Linker btw MCTruth to UTHits/UTTracks/UTDegits…

UT



UP



14 bits for module, and 20 bits for pixels

A 32-bit ID for HV-CMOS

- ➢ LHCb working on possibility to expand LHCbID container for upgrade II
- ➢ LV-CMOS channelID to be designed then

UP @ Gauss (Sim)

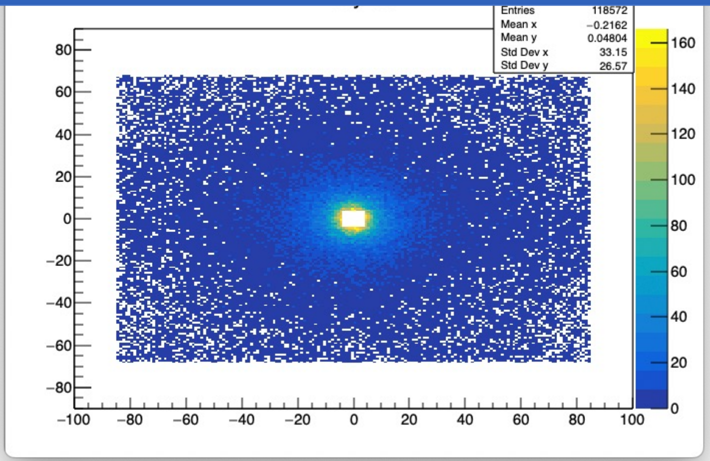
In DetDesc framework, UP detector geometry implemented into LHCb software via the interface so-called DetUP

- DetDesc gives G4Hits, transferred into MCHits with given new UTChannelID

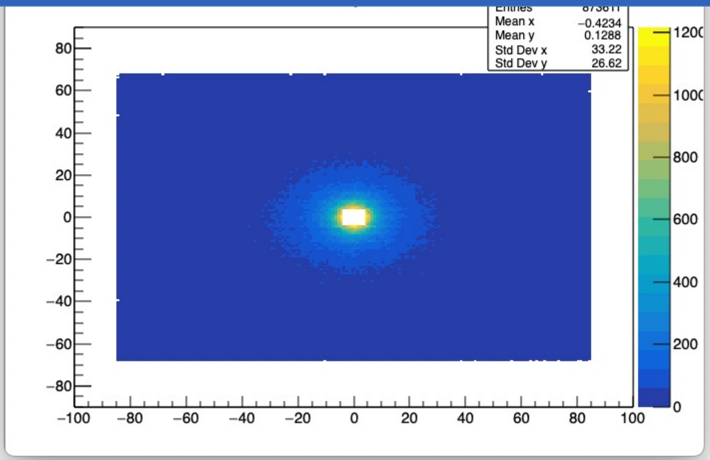
Tests for Gauss jobs

- Low or High luminosity samples generated in Run 3/4 or Run 5/6 condition
  - VP, SciFi and Magnet using as current one
- Gauss works for UP in DetDesc and DD4hep

MC Hits in 1st layer @ Run-3/4 condition



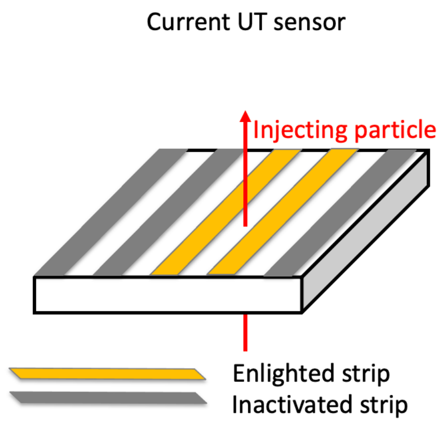
MC Hits in 1st layer @ Run-5/6 condition



UP @ Boole (Digit)

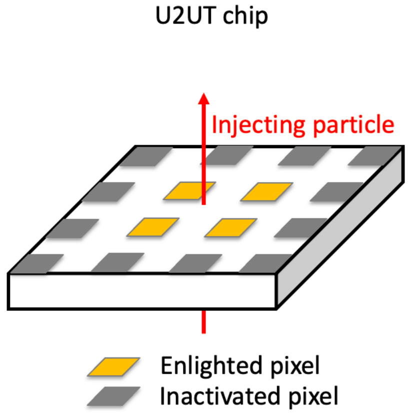
Digitization of UP pixel chips

- New algorithms for MCHits ⇒ deposit charges (UTDeposits) ⇒ UT ADC signals (UTDigits)
  - FE simulation parameters copied from current UT, can be updated from DB once more reliable numbers ready
- Written into RawBank via new encoder



Boole monitoring

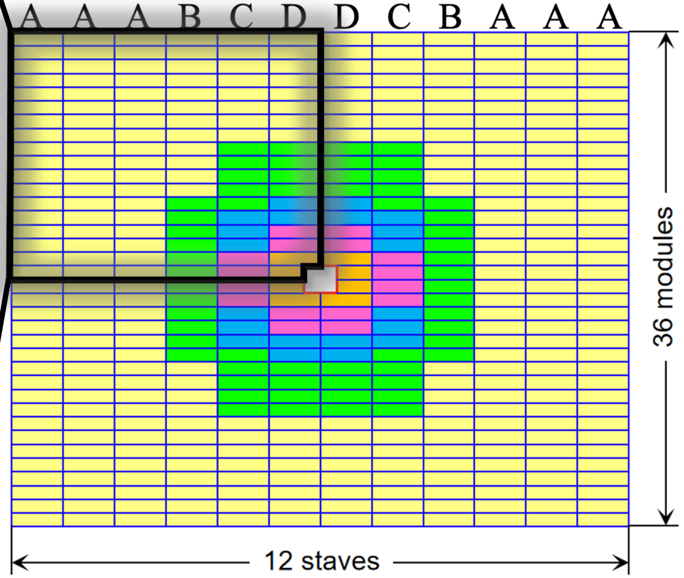
- Associating tables btw MCHits ↔ UTDigits and MCParticles ↔ UTDigits
- Efficiency calculator works
  - Response efficiency of MCParticle excited UTDigit (UT electronic signal)



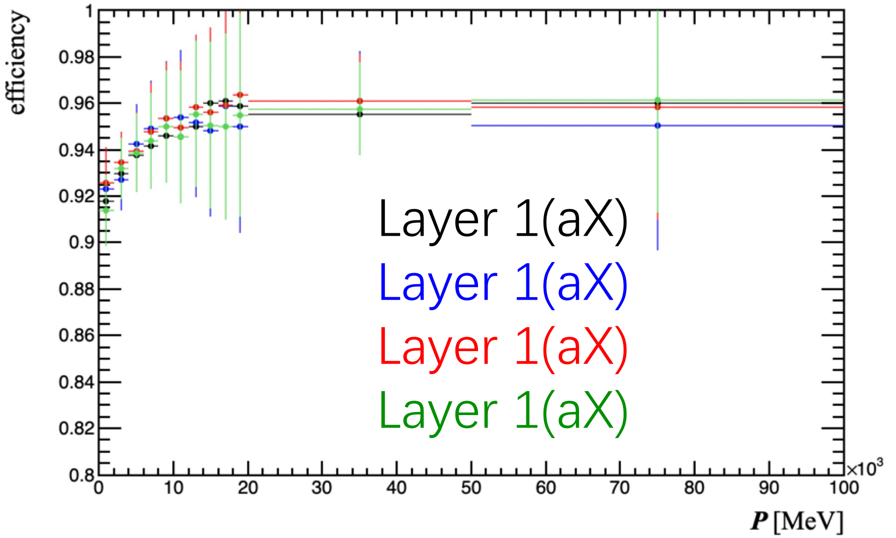
Studies @ Boole (Digit)

Averaged pixel occupancy (‰) on most busy chips of the modules

0.003	0.004	0.003	0.004	0.005	0.005
0.003	0.004	0.004	0.004	0.007	0.004
0.003	0.004	0.004	0.005	0.004	0.005
0.003	0.003	0.004	0.008	0.006	0.006
0.003	0.004	0.009	0.006	0.006	0.006
0.006	0.008	0.006	0.008	0.007	0.010
0.004	0.005	0.007	0.005	0.006	0.007
0.004	0.005	0.006	0.008	0.009	0.009
0.004	0.005	0.006	0.009	0.010	0.015
0.005	0.005	0.009	0.009	0.011	0.013
0.006	0.008	0.006	0.008	0.013	0.017
0.005	0.006	0.007	0.011	0.020	0.019
0.004	0.006	0.009	0.012	0.020	0.025
0.006	0.006	0.010	0.013	0.024	0.032
0.004	0.006	0.009	0.015	0.031	0.057
0.005	0.006	0.009	0.017	0.034	0.088
0.006	0.011	0.009	0.018	0.049	0.256
0.009	0.008	0.016	0.021	0.047	0.225



Particles response efficiency as a function of particle momentum per layer



Results @ Run5/6 condition

- Current (strip) UT has ~95%

- Hottest pixel occupancy estimated based on 1.2K miniBias MC events
- Consistent with estimation in FTDR

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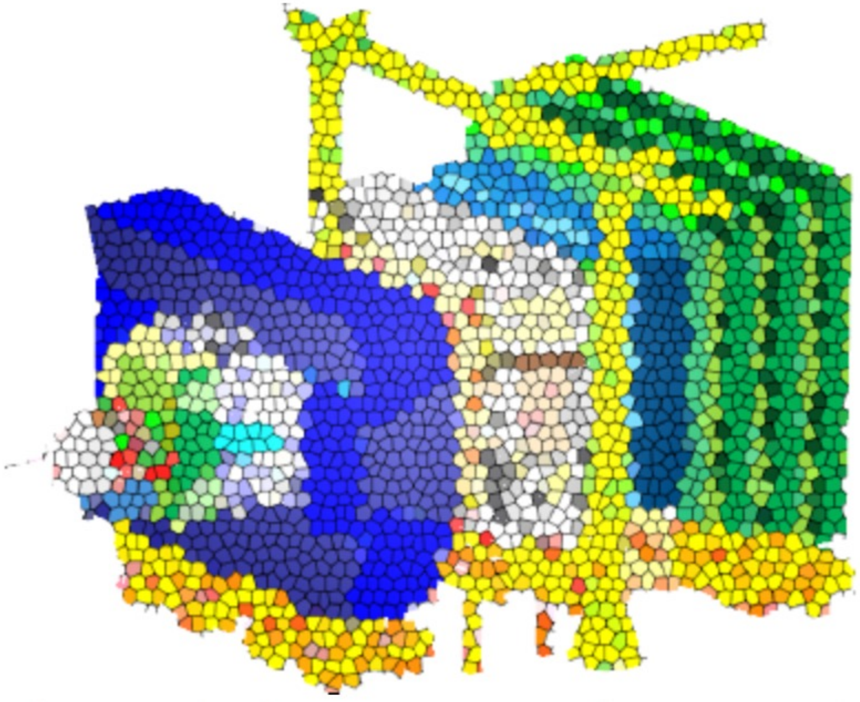
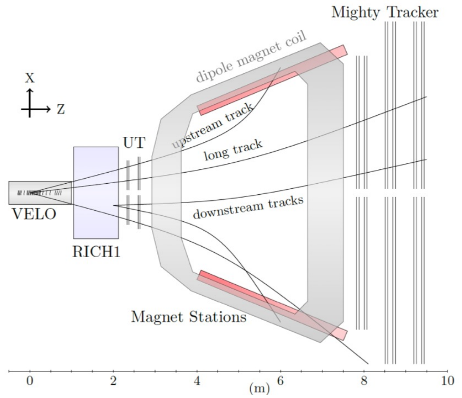


Tracking Efficiency

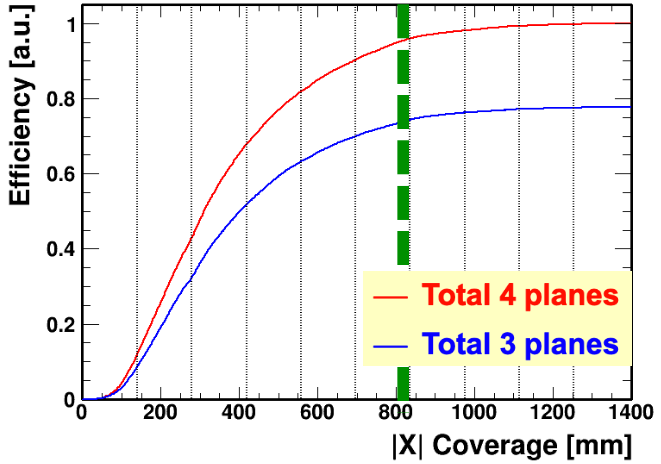
Track efficiency for interested processes studied for coverage optimization

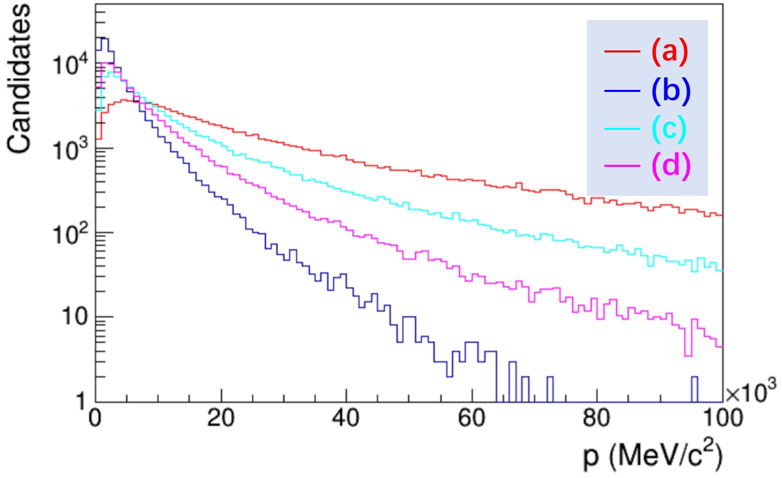
➢ $\bar{B}^0 \rightarrow D^{*+}\pi^-, D^{*+} \rightarrow D^0\pi^+, D^0 \rightarrow K_s\pi^+\pi^-, K_s \rightarrow \pi^+\pi^-$

(a) (b) (c) (d)



Track efficiency vs X coverage





Single Track With 3 UT Hits, |X| < 836.2 mm				
Requirement	(a)	(b)	(c)	(d)
Total 4 planes	96.2%	97.1%	96.2%	96.0%
Total 3 planes	91.3%	92.6%	91.3%	91.4%

Future plan

- More decays and particles to be used
- Decrease module/stave/layer to be studied
- Based on upgrade I UT software, need to port into full simulation software

Conclusion

UP simulation development processing well

- "Fake digitization": UP geometry ready
  - Try to merge our detector to the master branch
  - LHCb DD4hep still under developing, more communication required for LHCb simulation WG
- Full simulation: In both frameworks, UP can run in Gauss
  - Boole can also work in DetDesc framework
  - Pixel tracking algorithm developing now
  - More works ahead, but no interference with TDR studies
- Physics performance: Scoping studies will move on
  - Detector optimization to be studied
  - Real Upgrade 2 software for these studies in next step
- Regular meeting: https://indico.cern.ch/event/1342298/
- The goal is TDR by 2025

Thank you !

BACKUP

RawBank en/decoder

UP RawBank format built for software development

- ➢ **NOT for real, must be updated in future**
- ➢ RawBank encoder done @ Boole level
- ➢ The non-clustering decoder done @ Rec level
  - ❑ A smart iterator built to point to only interested positions in Bank

Example of a normal event

Event Header & Flags								Lane 5				Lane 4				Lane 3				Lane 2				Lane 1				Lane 0			
16b		16b		16b		16b		16b		16b		16b		16b		16b		16b		16b		16b		16b		16b		16b		16b	
8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b	8b
Event 0 Header								Hit1		Hit0				Hit0		Hit1		Hit0		Hit1		Hit0		Hit1		Hit0		Hit1		Hit0	
																		Hit2		Hit3		Hit2				Hit2					
																						Hit4									
										A1	A0				A0		A2	A1	A0	A3	A2	A1	A0		A2	A1	A0			A1	A0
																							A4								

Normal pixel hit

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Local Pixel ID [16b]															

Normal ADC hit

7	6	5	4	3	2	1	0
		ADC value [5b]					

Gray boxes for zero

Event header format

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Event ID from TFC [8b]								Reserve zero								Hits # in Lane 5 [8b]								Hits # in Lane 4 [8b]							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Hits # in Lane 3 [8b]								Hits # in Lane 2 [8b]								Hits # in Lane 1 [8b]								Hits # in Lane 0 [8b]							