

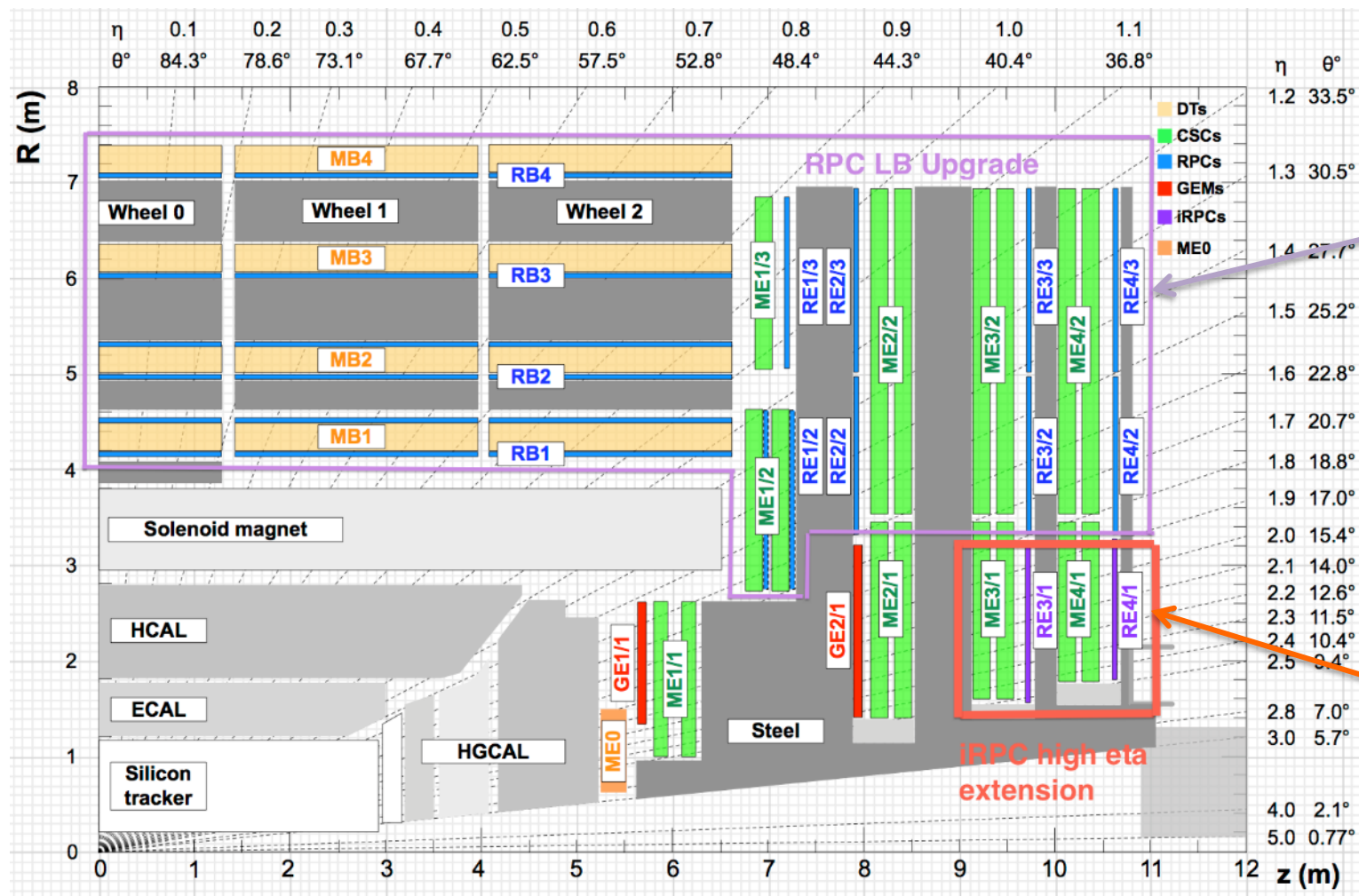
CMS iRPC Backend and Trigger status

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Trigger Lab/IHEP Beijing

CLHCP2023

- Overview
- iRPC BE/TRG demonstrator development
- Preliminary results of data analyses for beam test
- BE development for iRPC QC3
- P5 demonstrator backend integration preparation
- Summary

CMS Phase-II RPC Upgrade Overview



Upgrade of Link System to improve timing resolution for existing RPC ($|\eta| < 1.9$)

Extend the RPC coverage up to $|\eta| = 2.4$ to increase redundancy in high eta region in stations 3 and 4

iRPC/RPC backend and Endcap Trigger task

◆ iRPC BackEnd and Trigger (iRPC BE):

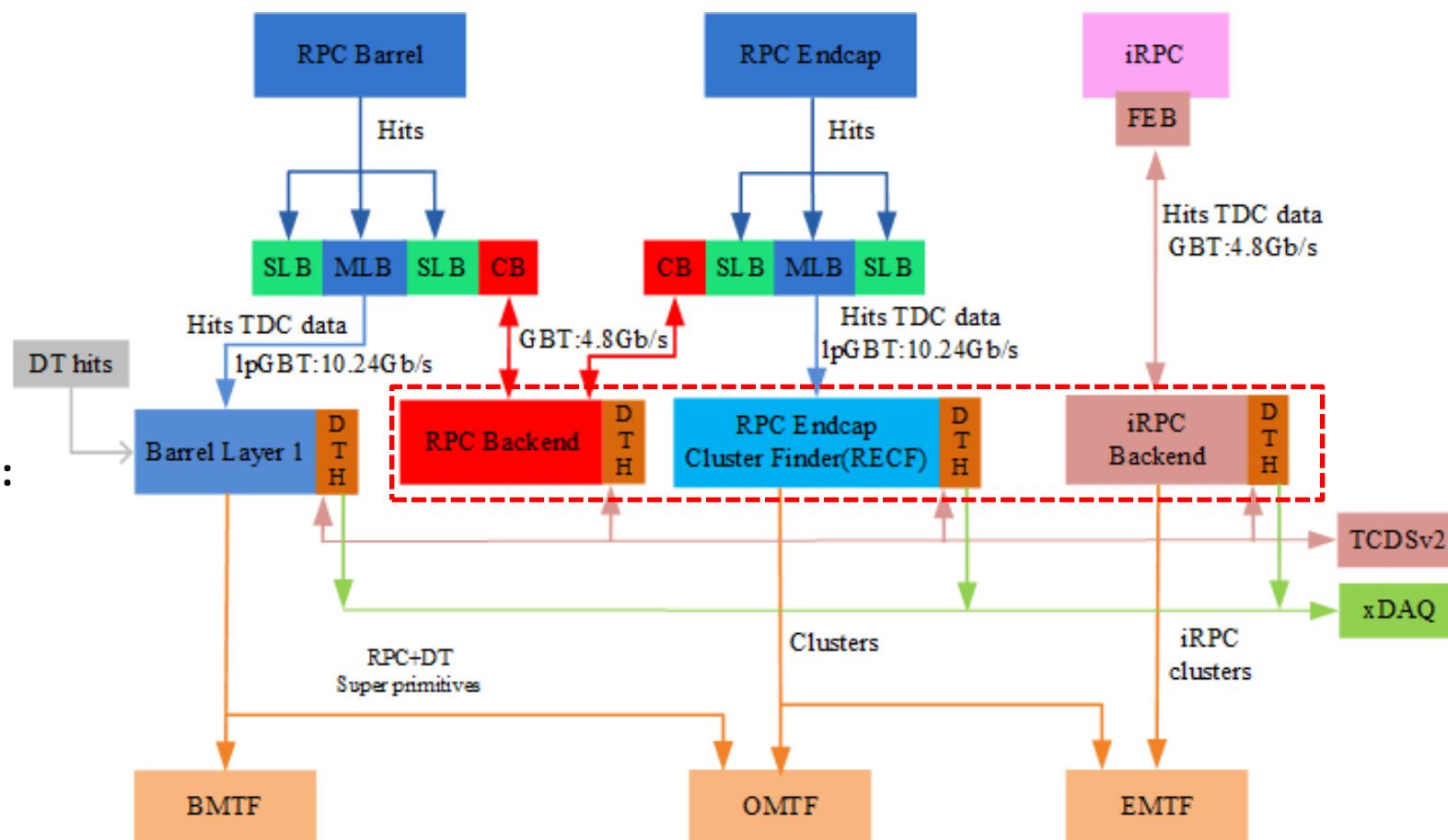
- Fast/Slow control(TTC),
- Monitor
- Data readout,
- Trigger Primitive(Cluster) Generation

◆ RPC Endcap Cluster Finder(RECF):

- Data readout
- Trigger Primitive(Cluster) Generation
- TP data Fanout

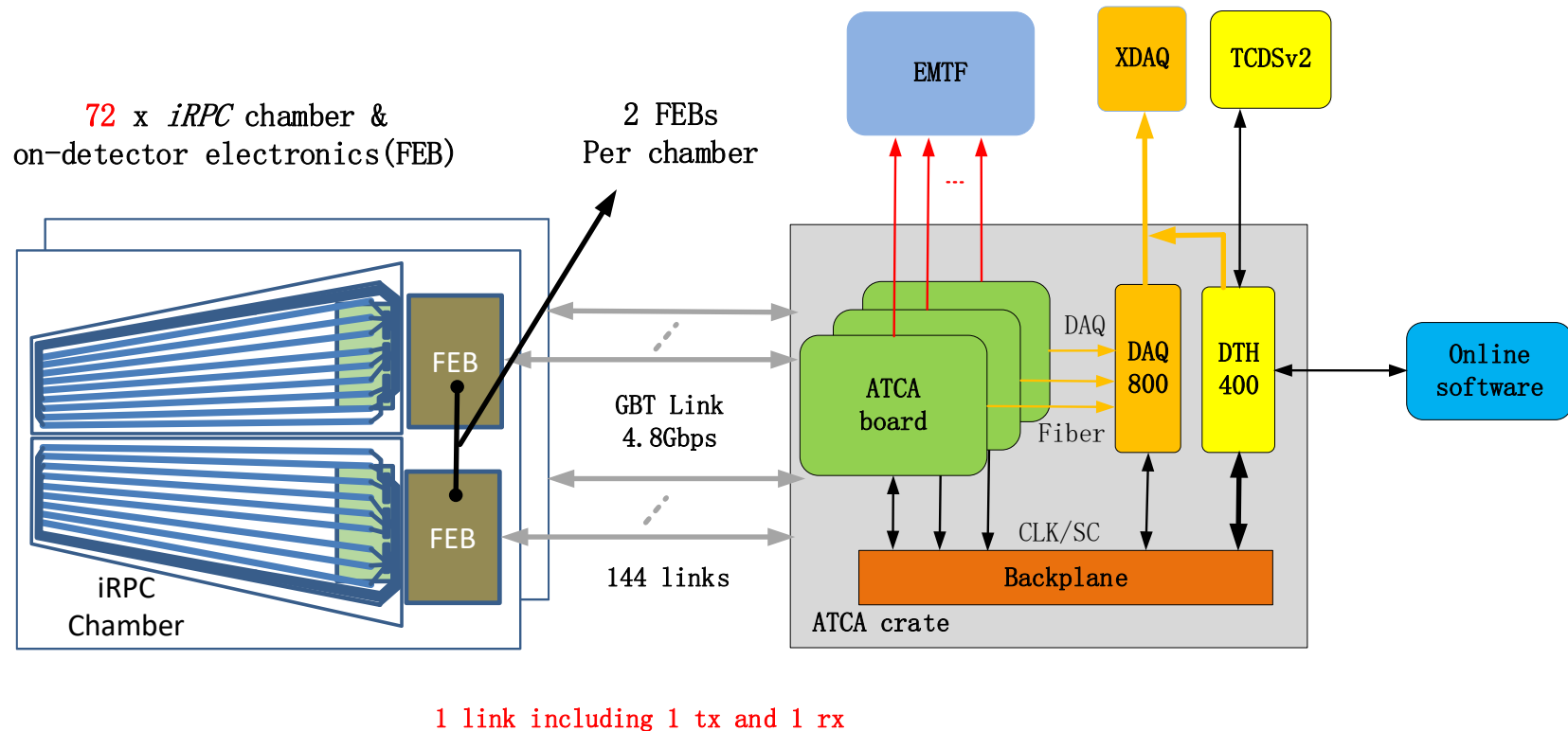
◆ RPC backend:

- Fast control(TTC)
- Slow control
- monitor



◆ iRPC BE/TRG system

- 1 ATCA Crate
- 1 DTH400
- 1 DAQ800
- 8 ATCA serenity boards



iRPC Backend and Trigger schedule

◆ 2023-2024

- MTCA BE/TRG integration in P5 on iRPC demonstrators with FEB V2_2
- Data taking in P5 use MTCA BE/TRG board for iRPC demonstrator chamber test
- work in Serenity steering committee and technical group for key technology design and test

◆ 2025 -2026

- Start BE/TRG firmware merge to serenity ATCA
- ATCA BE/TRG integration in P5 on iRPC demonstrators with FEB V2_3

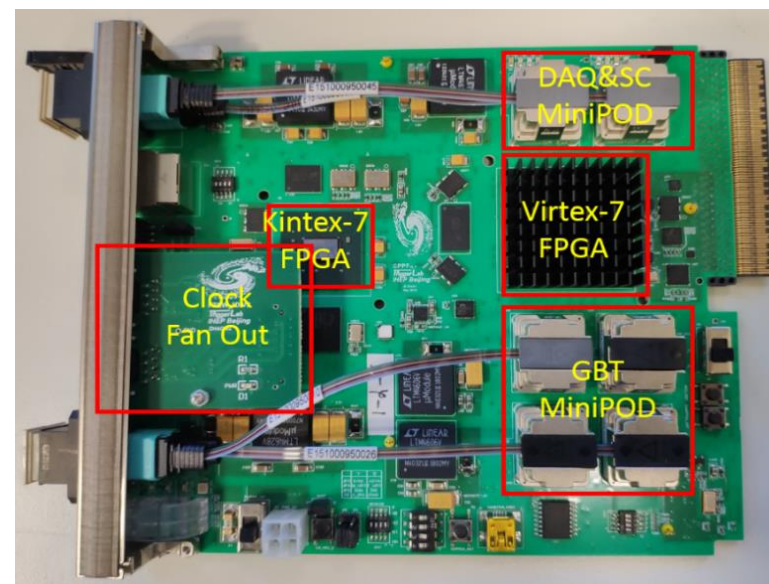
◆ 2027-2028

- Full ATCA BE/TRG for iRPC integration in P5
- Taking Data with iRPC chamber installed in P5 in local

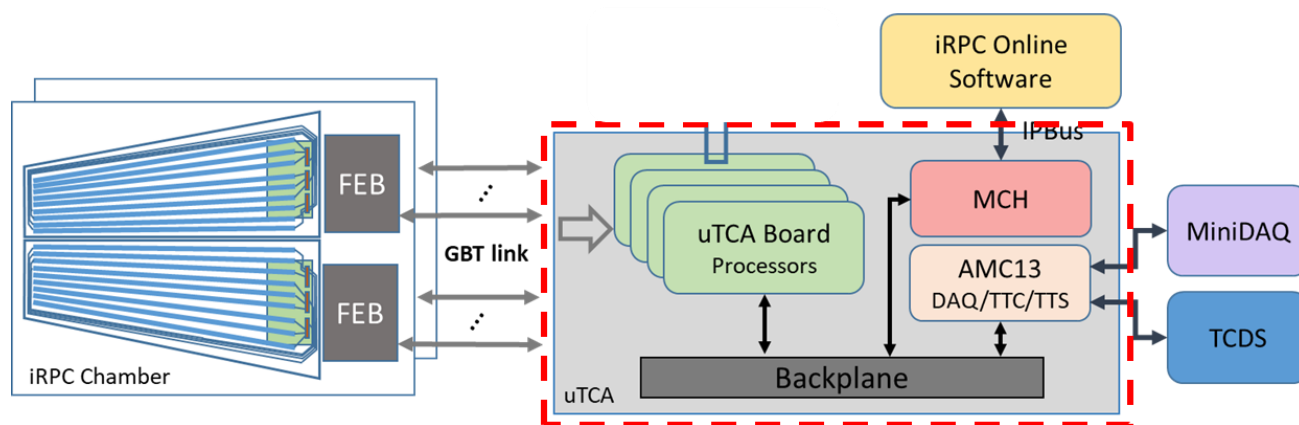
iRPC Backend and Trigger progress

- ◆ Present progress is based on MTCA BE board.
 - iRPC BE/TRG firmware development, online control function integrated
 - Suggestion to FEB for firmware upgrade based on beam test
 - Timing reference study
 - Backend system setup and development for QC3 in Gent, Mexico and 904
 - iRPC P5 demonstrator backend integration preparation
- ◆ Details of progress see following slides.

- Before Last version of ATCA serenity board availability, we are working on present BE/TRG board for system study.
- BE/TRG board-designed by IHEP trigger group
 - Virtex-7 FPGA: Core FPGA(GBT Communication with Feb + data processing);
 - Kintex-7 FPGA: Control FPGA(clock configuration , SC)
- iRPC BE/TRG Demonstrator

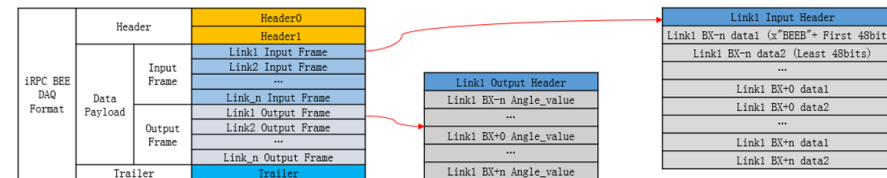
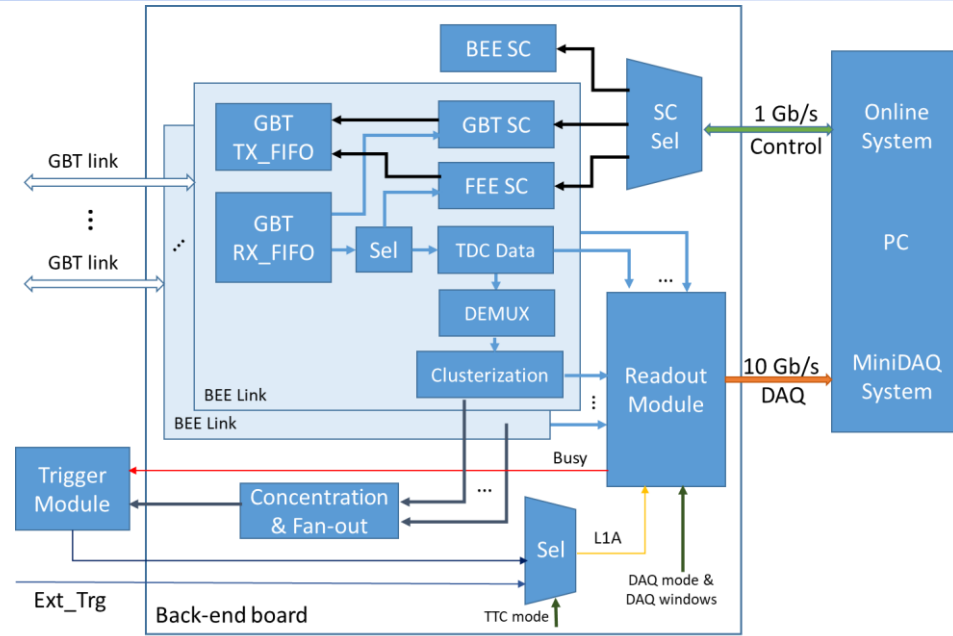


System in Beijing similar to the one in P5



Currently iRPC BE function design progress

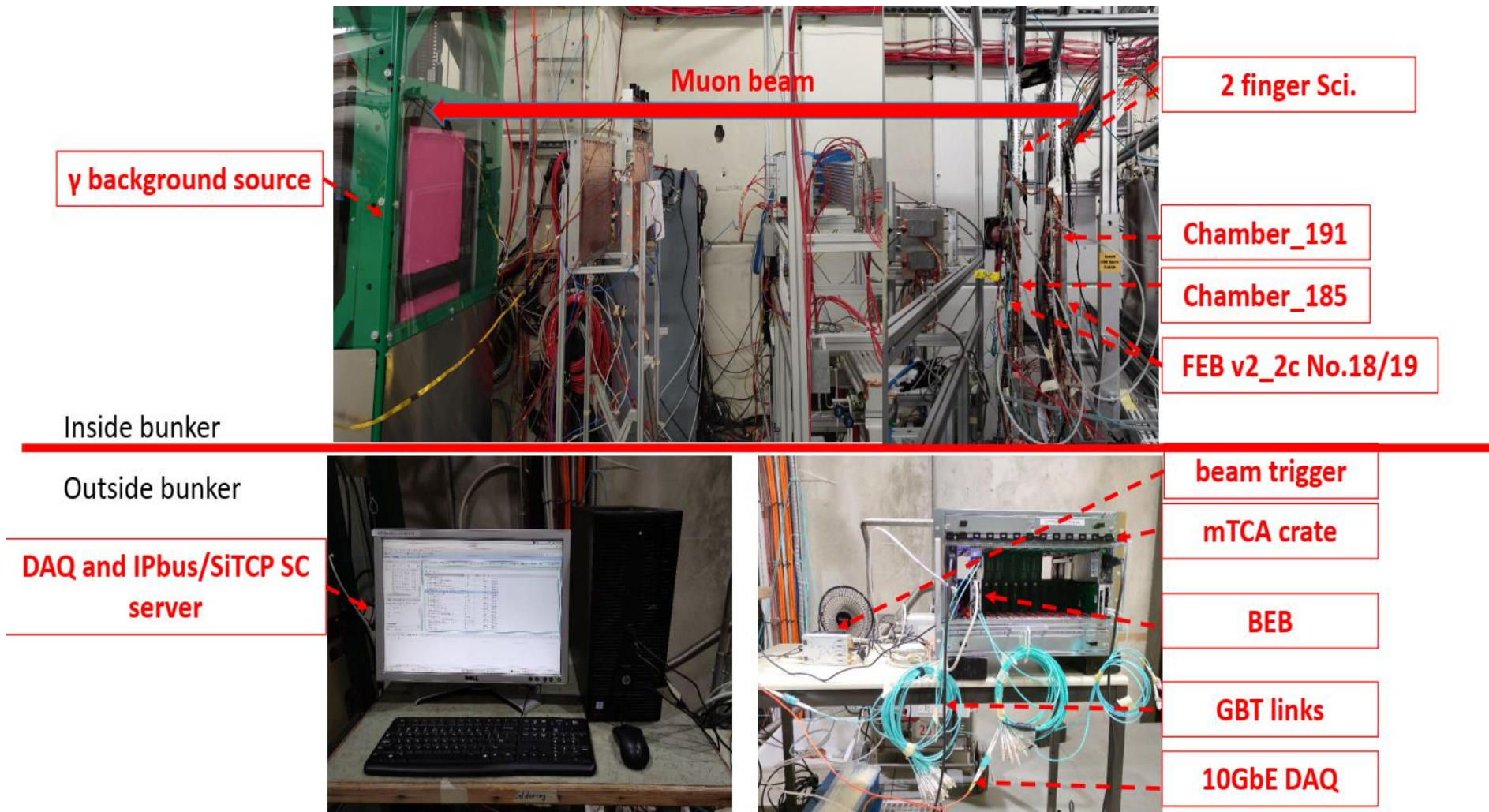
- BE firmware function
 - Transmission link: **Done**
 - Bidirectional, 4.8Gb/s
 - Fast control: **Done**
 - BC0/resync
 - Timing reference distribution
 - Slow control: **Done**
 - BEE-SC/FEE-SC/GBT-SCA
 - PC to BEB control link
 - 1Gb/s, Sitsp protocol/Ipbu
 - Cluster finding algorithm: July 2024
 - DEMUX/Cluster finding/Angle conversion
 - DAQ package: May 2024
 - BEB to PC DAQ link : **Done**
 - 10Gb/s, TCP/IP



	Byte 7	Byte 6	Byte 5	Byte 4	Byte 3	Byte 2	Byte 1	Byte 0
Header0	Special Mark ("DEADBEF")				Trigger Number			
Header1	Orbit Number				Event Length			
Input Link Header	LinkType ("FA")	Link8 Length (7b)	Link7 Length (7b)	Link6 Length (7b)	Link5 Length (7b)	Link4 Length (7b)	Link3 Length (7b)	Link2 Length (7b)
Output Link Header	Link Type ("FFFF")	Link8 Length (6b)	Link7 Length (6b)	Link6 Length (6b)	Link5 Length (6b)	Link4 Length (6b)	Link3 Length (6b)	Link2 Length (6b)
Input Link Data	Uplink frame between the FEB and the BEB							
Output Link Angle value	1st cluster Theta(R value)		1st cluster Phi		2nd cluster Theta(R value)		2nd cluster Phi	
Trailer0	FSM Error	Link8 Error	Link7 Error	Link6 Error	Link5 Error	Link4 Error	Link3 Error	Link2 Error
Trailer1	Boo3_ID	BEE_version	CRC-32				Event Length	

Beam test in GIF++

- ◆ Data taking with beam for BE/TRG function development and verification .



2023 BE beam test result

◆ Purpose:

- Check new functions implemented in FEB firmware v3.6 and v3.15
 - the Check-Sort-Push(CSP) mechanism
 - Data send priority based on timing, not channel
 - HR and LR data pair function
 - (one strip tdc data from HR and LR concentrate in one GBT frame, and throw away only have HR or LR tdc data)

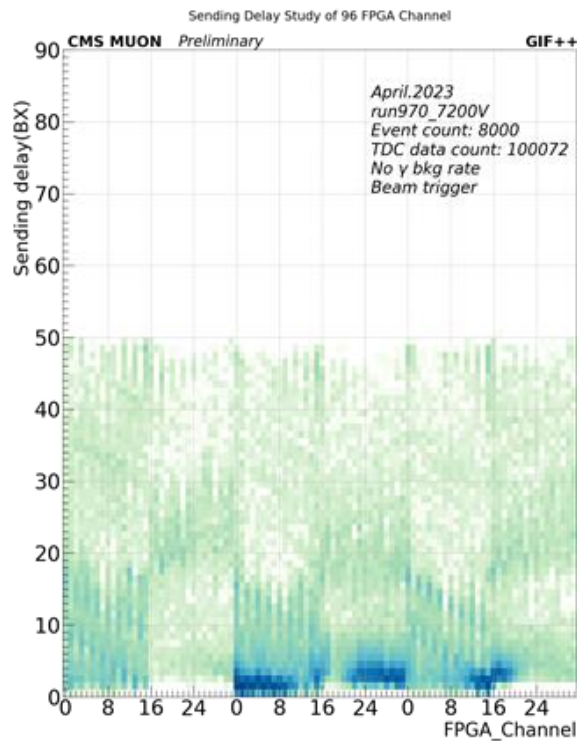
◆ Two kinds of Data took,

- pair function disabled
- pair function enabled

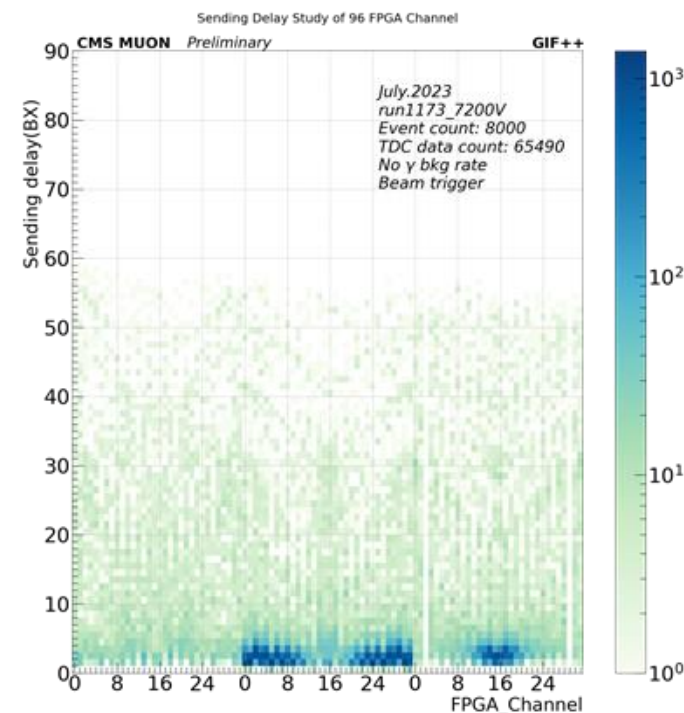
◆ Results:

- Data sending delay distribution meet expectation. More details under study.
- Give upgrade suggestion to FEB team on v3.6.
- Pair function enabled data as expected in v3.15.

Details refer Weizhuo's report: Data analysis for iRPC BE/TRG, <https://indico-tdli.sjtu.edu.cn/event/1616/contributions/9012/>



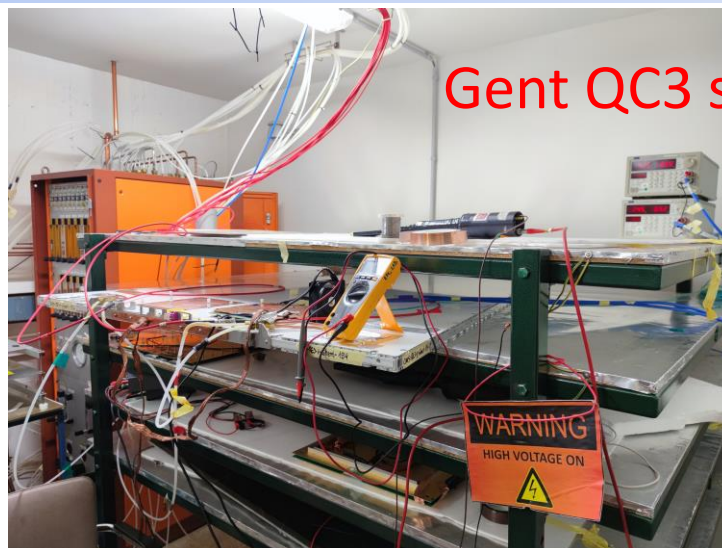
pair function disabled,
no gamma background



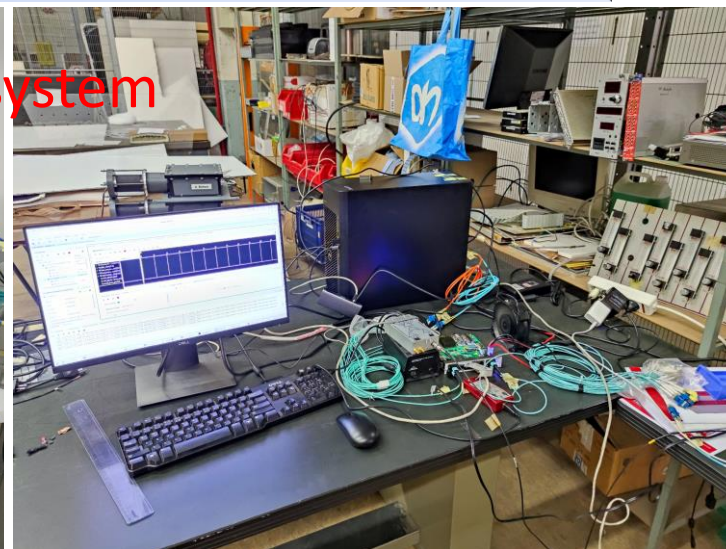
pair function enabled,
no gamma background

iRPC QC3 BE development

- ◆ QC3 - iRPC Chambers Quality Control
Chamber during construction and with cosmoics @ **assembly sites**: Gas leak, dark current, cosmic (noise, eff, cluster size, HV).
- ◆ iRPC QC3 backend system.
 - Based on BE/TRG demonstrator
 - Single board system
 - One board readout one FEB for half chamber.
- ◆ Developed and set up two systems
 - Gent system: Jianing helped set up this system in July.2023
 - 904 system: Qingfeng set up 904 backend system



Gent QC3 system

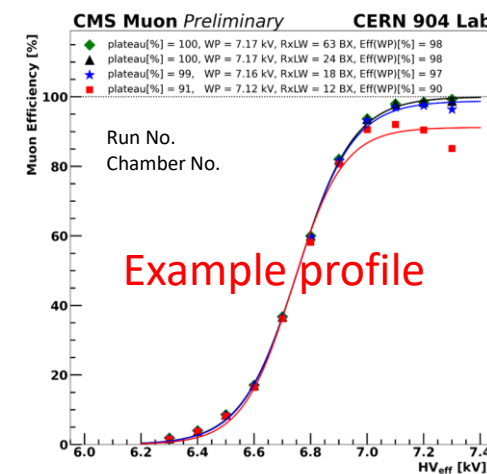
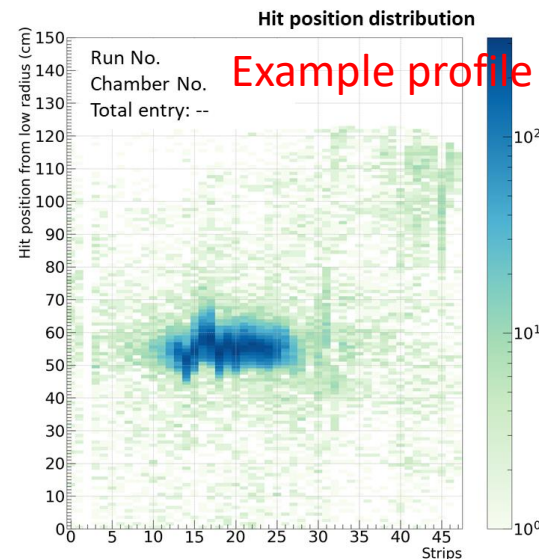
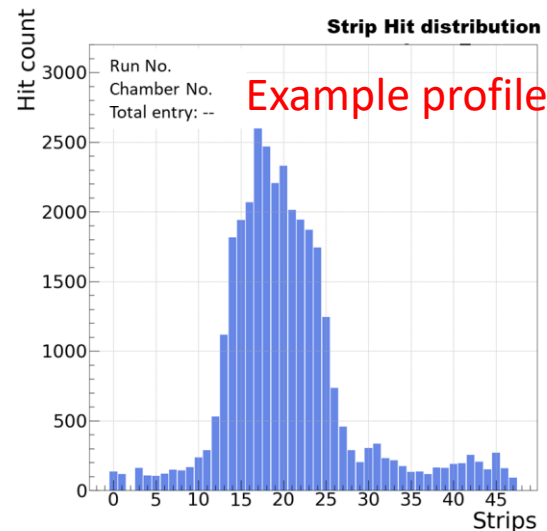
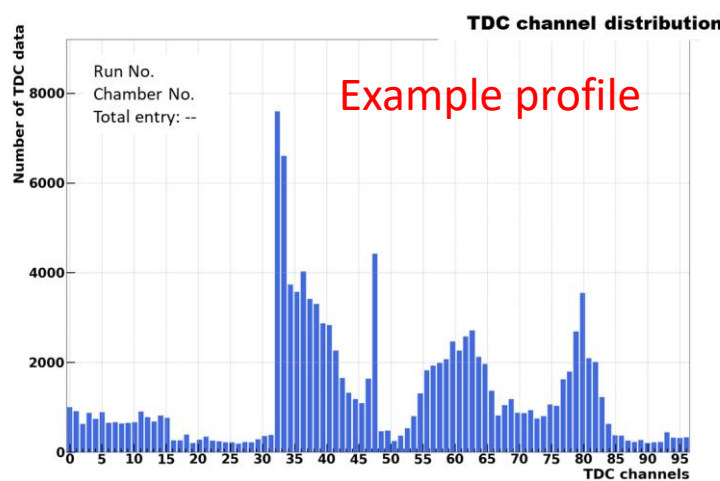


904 QC3 system



iRPC QC3 BE development

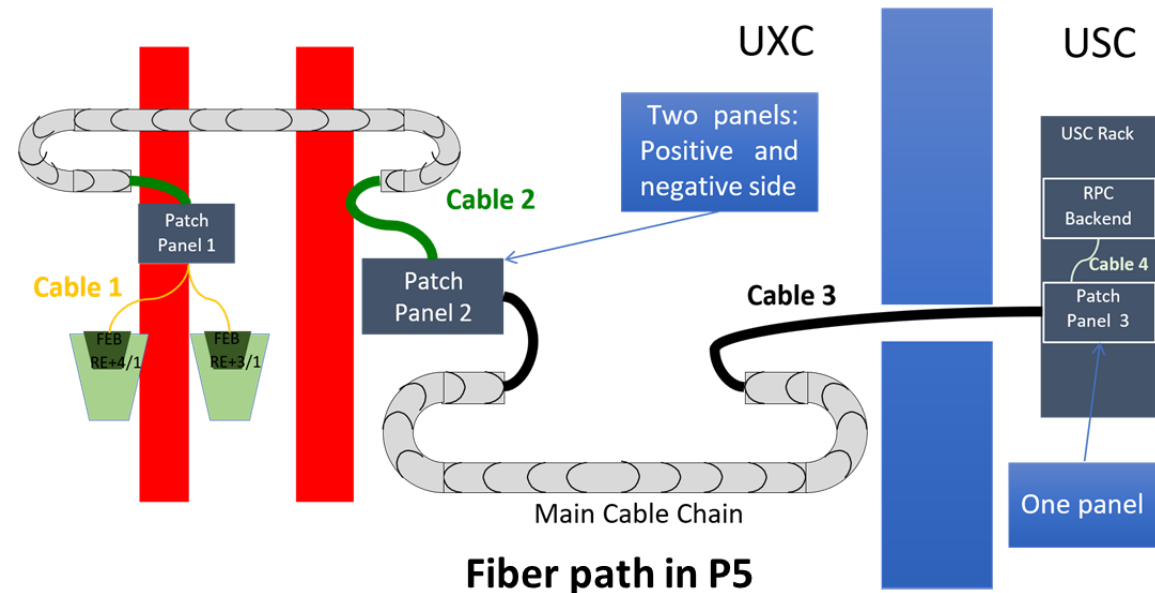
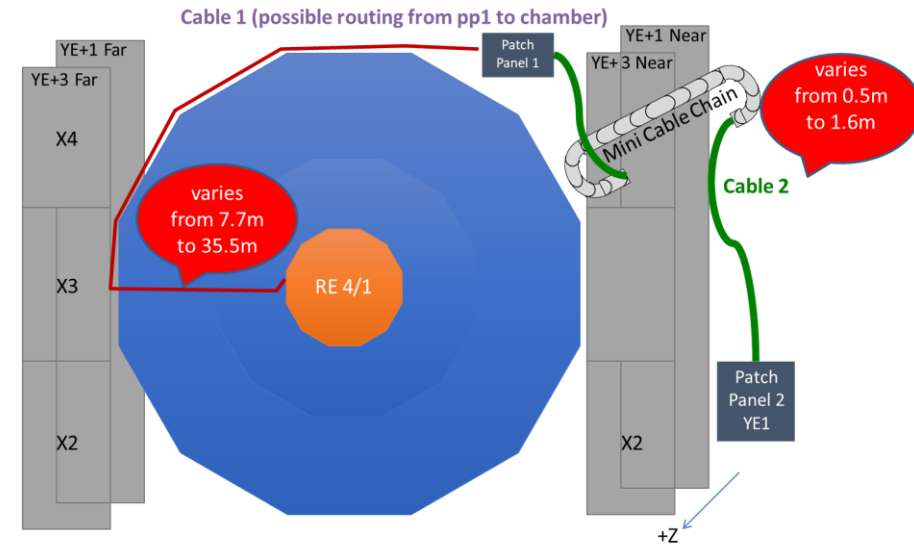
- ◆ Qingfeng is working on QC3 data analysis module for quick test, 3 kinds of profile will generate after each QC data taking.
 - TDC channel distribution: used to check is there any dead strip channel.
 - Strip Hit distribution: used to roughly check FEB/BE working status and SCI area correct or not.
 - Hit position distribution: roughly check SCI area is correct or not.
 - How to provide the s-curve line is still under discussion.
- ◆ These modules will be integrated in webdcs.



Fiber length affect on cluster finding study

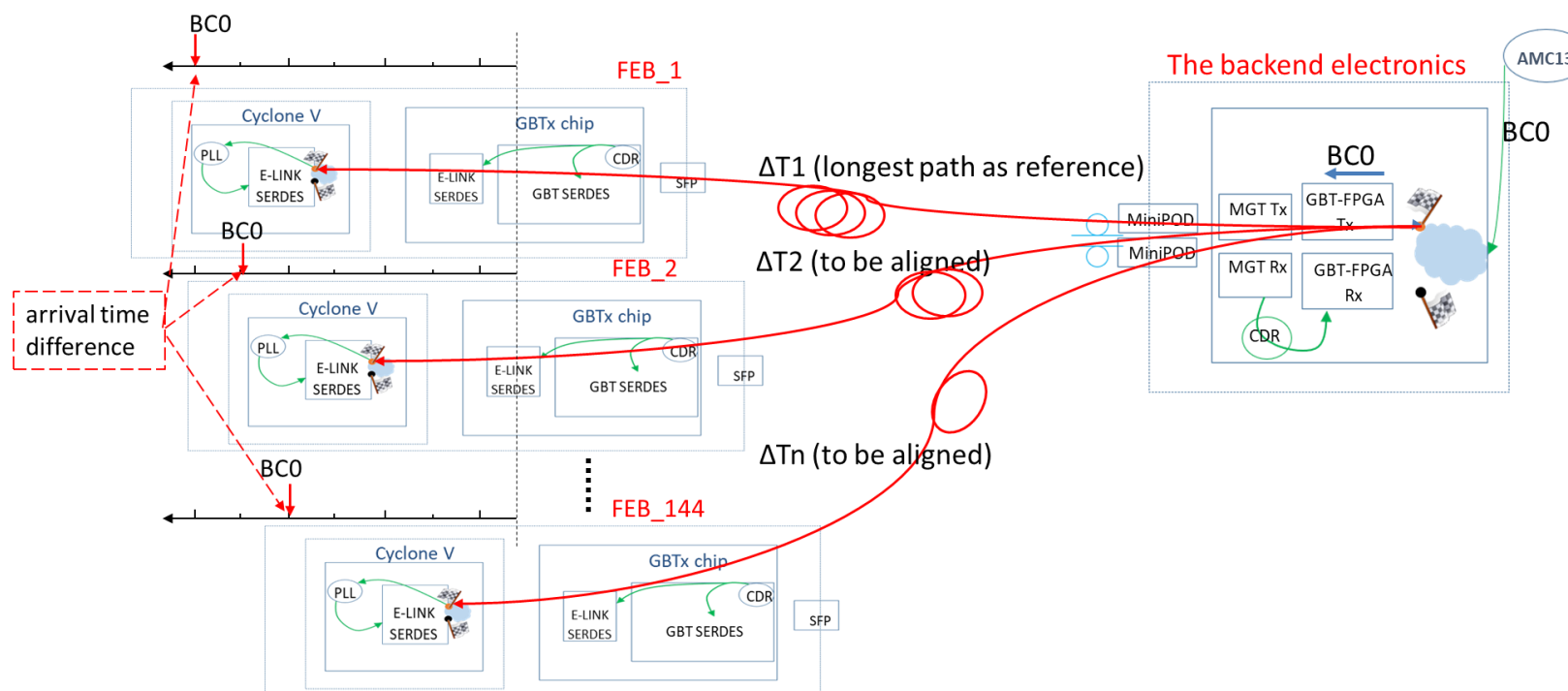
Chamber location and fiber cable routing

- Fiber Length (single direction):
 - Cable1 : varies from 7.7m to 35.5m
 - Cable 2: varies from 0.5m to 1.6m
- Maximum fiber length difference is 28.9m roughly.

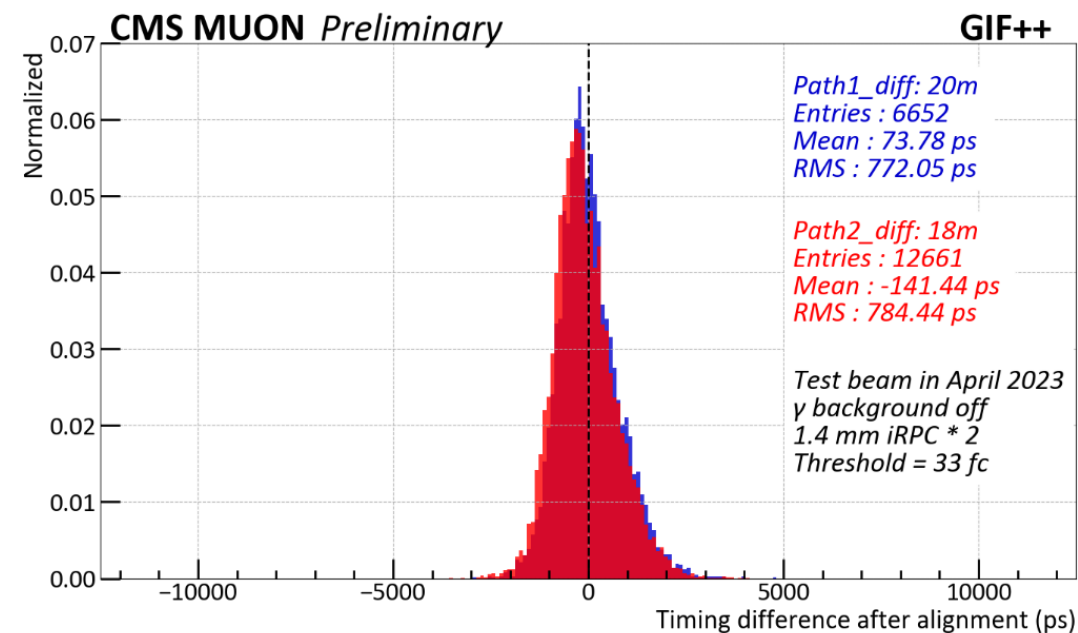
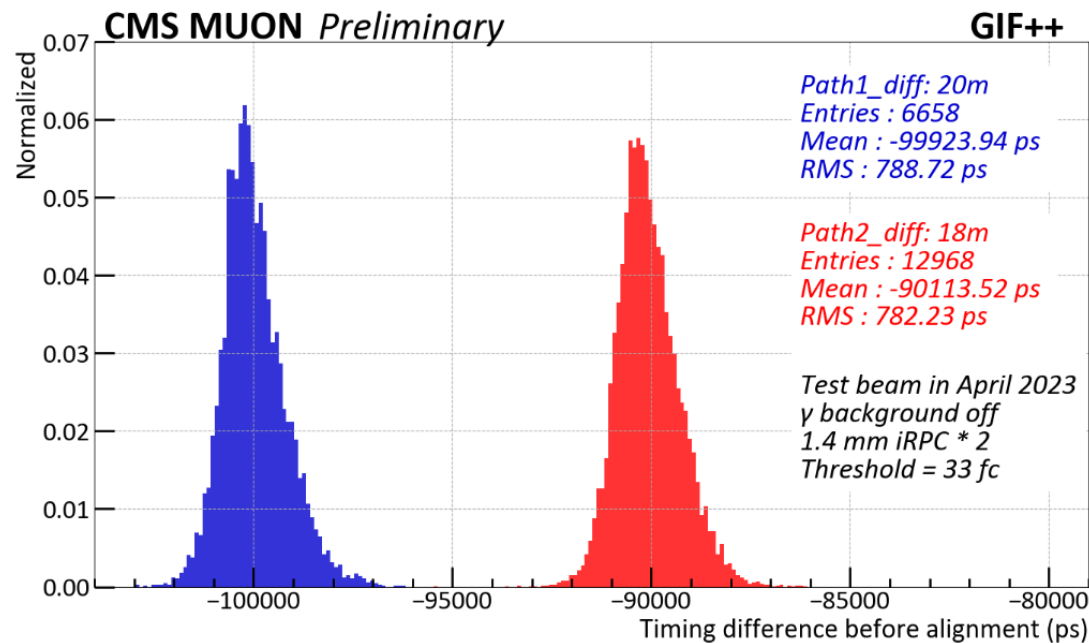


Fiber length affect on cluster finding study

- ◆ iRPC chambers/FEBs receive fast control signal from backend via fiber cables,
 - Clock, bunch info. BCO
- ◆ Different timing reference arrival time for each FEB because of chamber different locations in CMS.
 - 28.9m roughly => leading to **144.5ns($\approx 6BX$)** absolute timing difference (speed 20cm/ns).
- ◆ Data in same event will have different timestamp. This make problem in cluster finding. This studied and compensated in BE.



Timing reference study result



- 3 channels system used for study, with fiber length 20m, 22m, and 40m.
- After alignment, Timing reference difference changed from -99.923/-90.115 ns to within 1.25 ns.

P5 Demonstrator BE/TRG integration plan

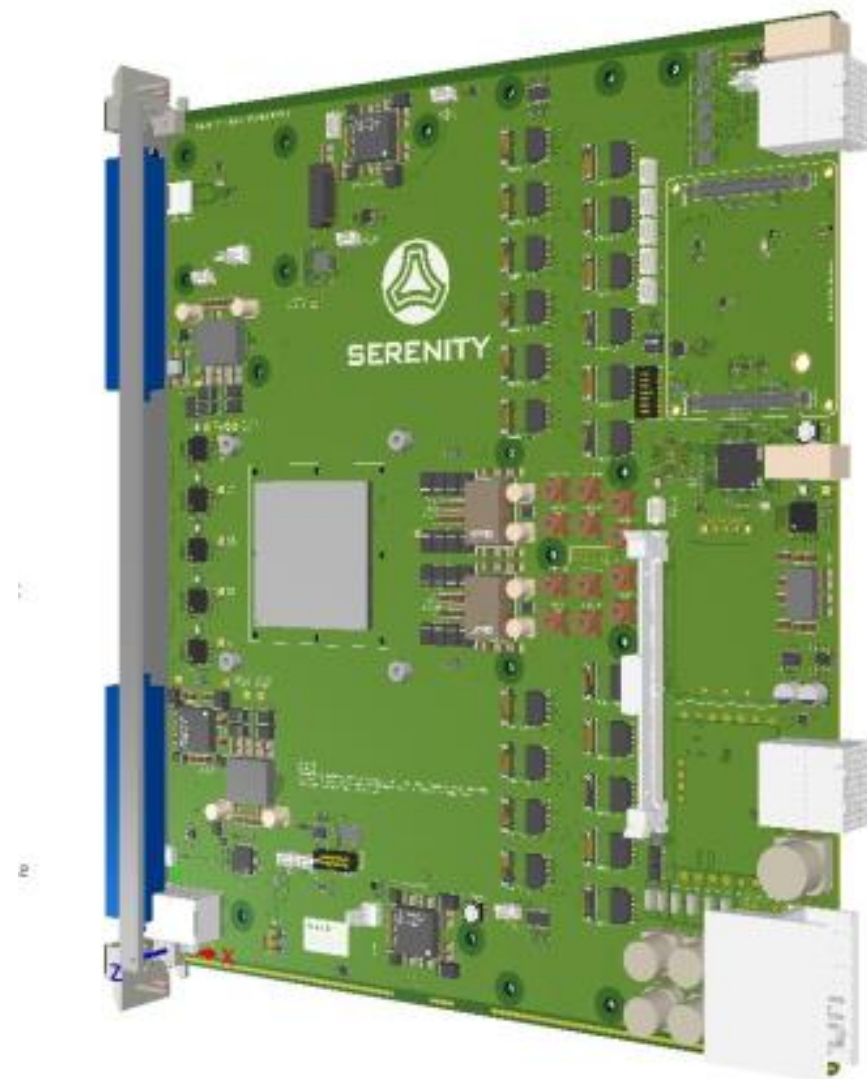
- ◆ P5 Demonstrator BE integration for iRPC schedule
 - Target 1, Nov. 2023: One BE/TRG board read two FEB boards without AMC13
 - Sitcp Slow control interface
 - Without MTCA crate and AMC13
 - Random trigger for noise data taking and self-trigger for data taking
 - Data taking and saving locally.
 - Target 2, Jan. 2024 : two BE/TRG board read four FEB boards with AMC13
 - Ipbus Slow control interface
 - With MTCA crate and AMC13, AMC13 working loopback mode
 - Random trigger for noise data taking and self-trigger for data taking
 - Data taking and saving locally.
 - Target 3, Spring 2024: Two BE/TRG boards read four FEB boards with AMC13 and CMS trigger (TBD)
 - Ipbus Slow control interface
 - With MTCA crate and AMC13, AMC13 connected with central TCDS
 - CMS trigger for data taking
 - Data taking and saving locally.

◆ Demonstrator integration preparation status

- One BE/TRG board is already in 904, so everything is ready for target 1 integration
- Another two BE/TRG boards are ready in Beijing lab, waiting for delivering.
- TTC module and DAQ readout module for two backend boards still under development.
- AMC13 configuration is being studied.

Status of ATCA Serenity

- ◆ Zhen-An LIU in Serenity Steering committee.
- ◆ Jingzhou ZHAO in Technical and Layout Group.
 - Schematic design
 - PCB layout and review
 - Serenity test
- ◆ Serenity-S1 version main function list.
 - Single FPGA design(Serenity-S1), Supports VU13P-A2577 package,
 - 124 bi-dir links @25 Gbps
 - Soc for board management.
- ◆ Serenity short plan
 - Serenity in pilot production
 - First small batch expected finish at the end of 2023.



Summary

- ◆ IHEP TRG group made good progress on iRPC/RPC BE/TRG this year.
- ◆ iRPC BE/TRG demonstrator developed for iRPC backend system study.
- ◆ iRPC data sending delay studied in beam test.
- ◆ Backend developed iRPC QC3 backend system and set up two system in Gent and 904.
- ◆ P5 backend Demonstrator installation is in preparation status.