Timing Readout Electronics Design with PETIROC2B to T-SDHCAL

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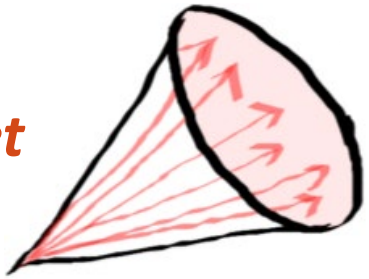
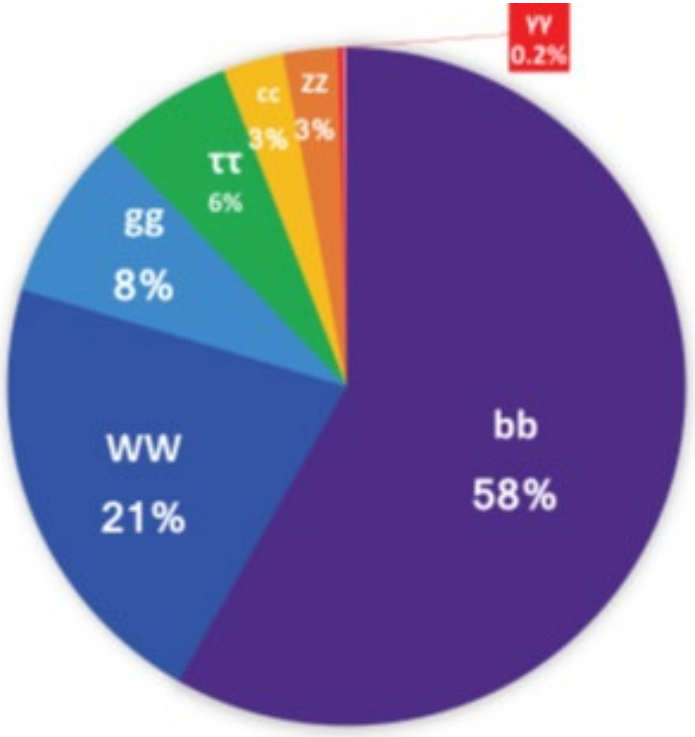
Outline

- Why high granularity calorimeter needed ?
- Particle Flow Algorithm and calorimeter
- Introduction of SDHCAL prototype
- Motivation of using timing information
- 5D T-SDHCAL with timing electronics design
- Summary

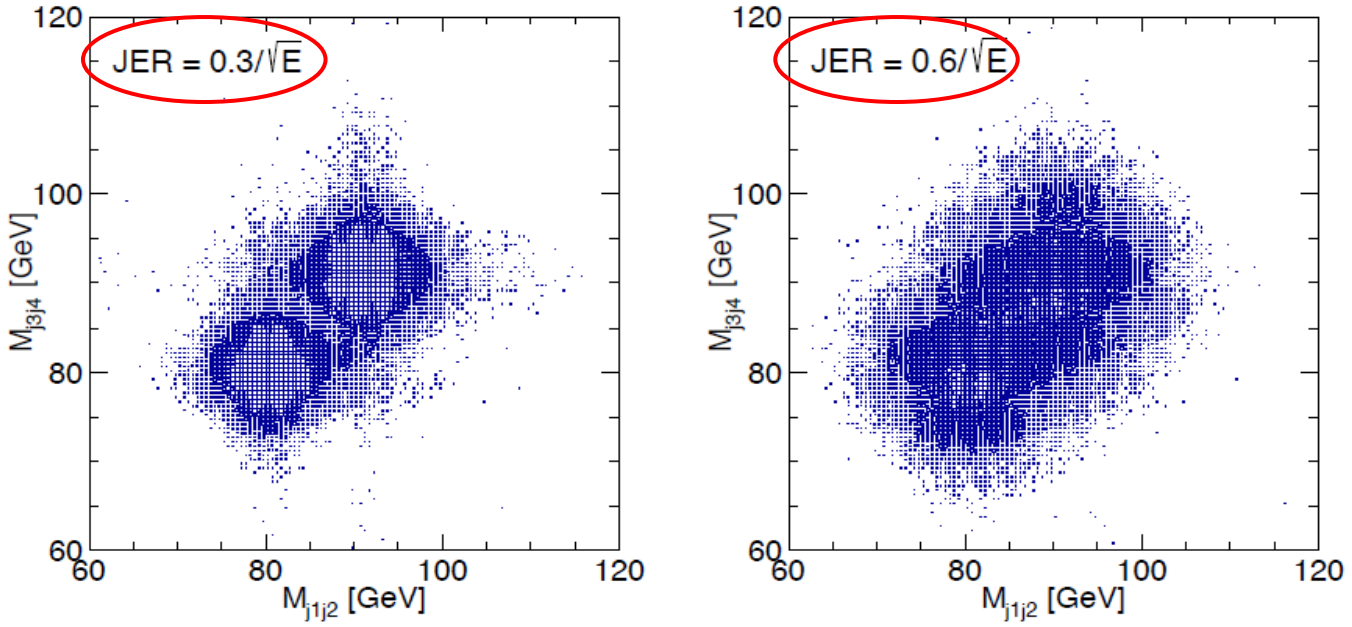
Why high granularity calorimeter ?

- ~70% of Higgs directly decay to a pair of jets
- ~20% of Higgs indirectly decay to jets
- ~70% of heavy boson (W, Z) decay to hadronic final states





Higgs Decay Final States

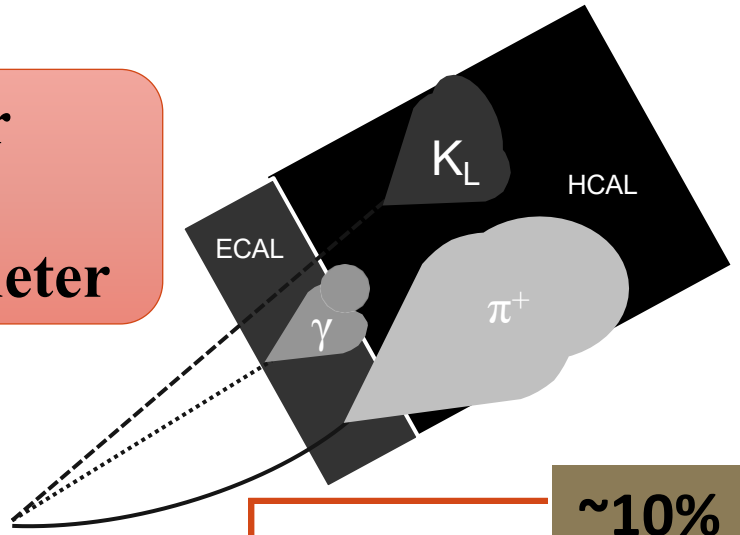


Jet Energy Resolution is important

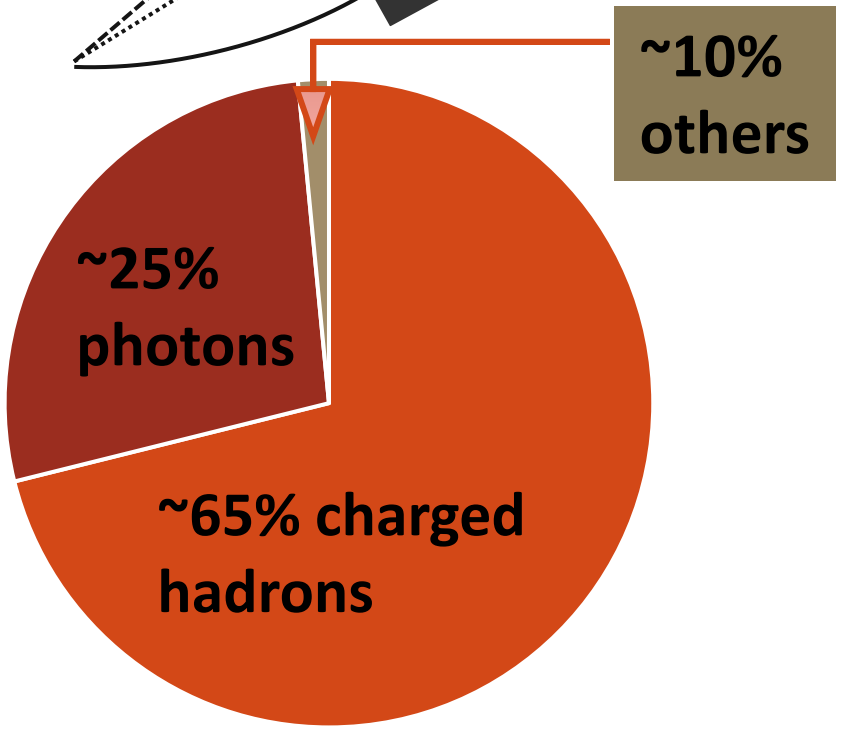
Particle Flow Algorithm (PFA)

Charged Particles } **measured with the** { **Tracker**

Neutral Particles } **measured with the** { **Calorimeter**



- The energy of a hadronic jet:
  - **~65%** charged hadrons (mostly pions)
  - **~25%** photons (mostly from π^0 decays)
  - **~10% neutral hadrons**



- Improve the jet energy resolution
- **Explicitly reconstruct neutral hadrons**
- **Reconstructing each final state particle(ideal)**
- **Combining the information of all subdetectors**

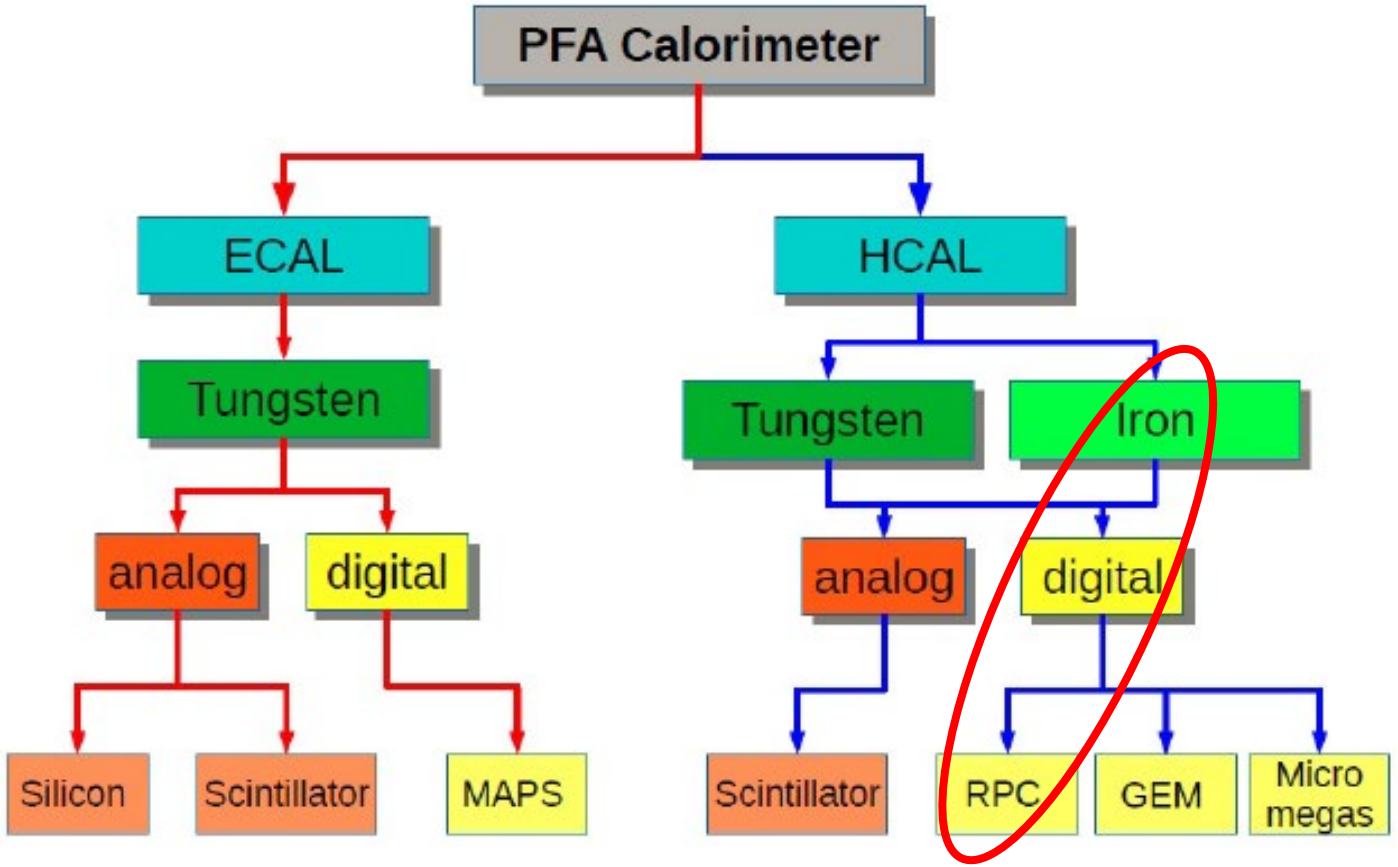
Calorimeter based on PFA

- **High granularity** calorimeter based on **Particle Flow Algorithm** has been proposed and verified.

Absorber :

Readout:

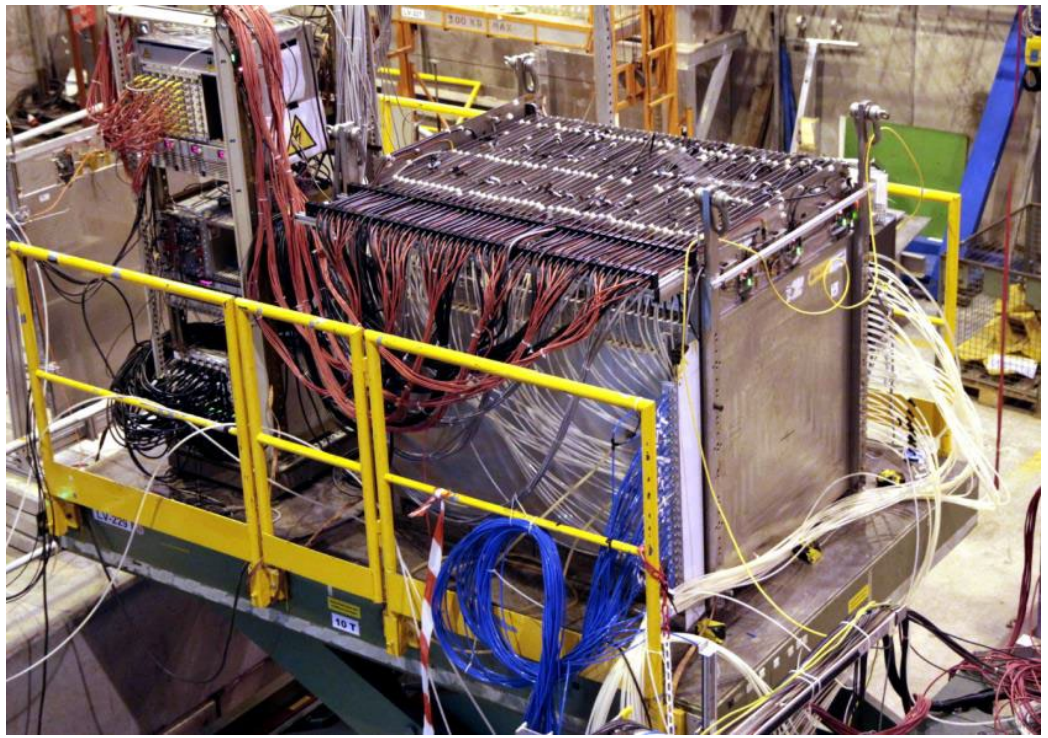
Active:



https://twiki.cern.ch/twiki/bin/view/CALICE/CalicePapers

Introduction of SDHCAL

- **S**emi-**D**igital **H**adronic **CAL**orimeter technological prototype.
- **High granularity** calorimeter based on **Glass RPC → Gas Chamber Detector**.
- **Hits associated to three thresholds**:
  - 1st threshold = 110fC
  - 2nd threshold = 5pC
  - 3rd threshold = 15pC

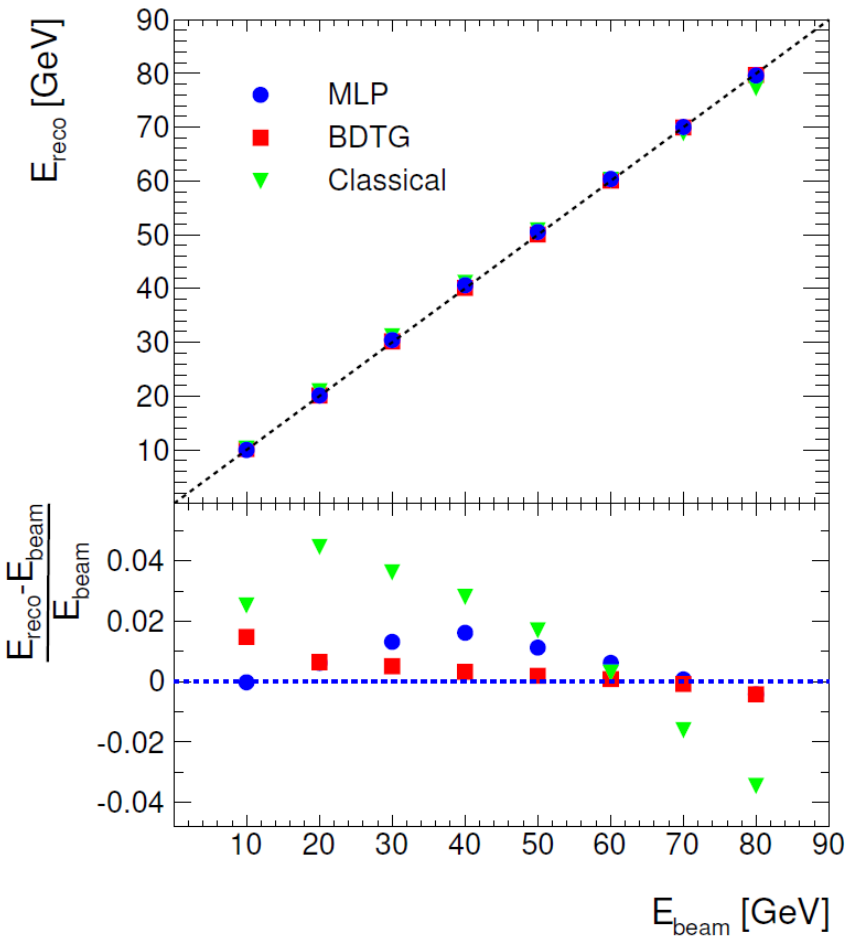


- 48 layers with GRPC as sensitive medium
  → Dimensions: 1m x 1m x 1.3m,
- 6 Interaction length ($\boldsymbol{6\lambda_I}$)
  → Semi-digital readout (0, 1, 2)

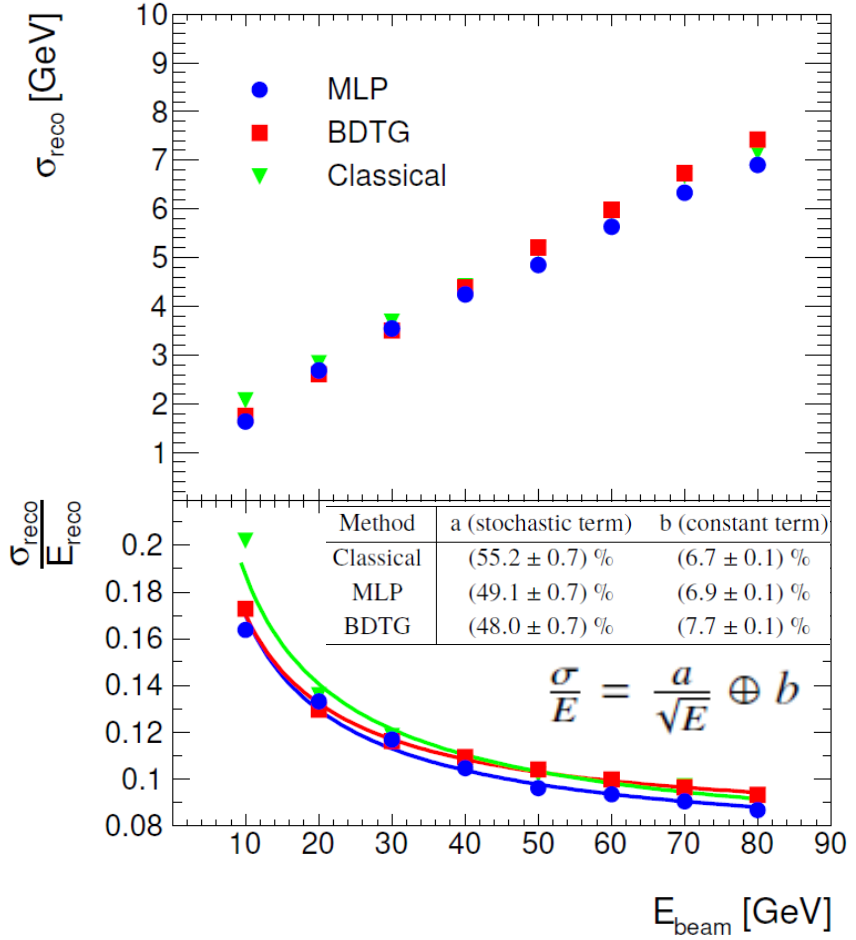
SDHCAL: energy linearity and resolution

JINST 14 (2019) 10, P10034
JINST 15 (2020) 10, P10009

Energy linearity improves from 3-4% to 1-2% level using MVA



Energy resolution relatively improves about 5-15% using MVA

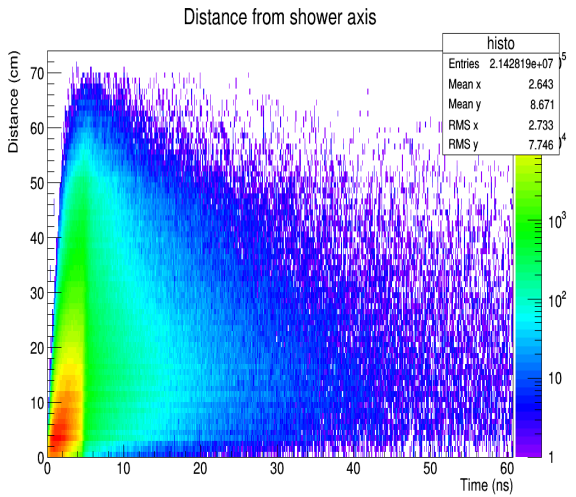


Method	a (stochastic term)	b (constant term)
Classical	(55.2 ± 0.7) %	(6.7 ± 0.1) %
MLP	(49.1 ± 0.7) %	(6.9 ± 0.1) %
BDTG	(48.0 ± 0.7) %	(7.7 ± 0.1) %

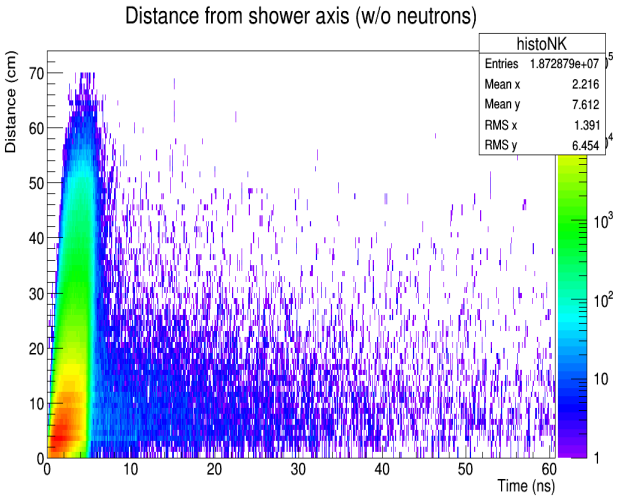
Motivation of timing

- SDHCAL has been performed the beam test since 2015 to achieve good energy reconstruction and particle identification.
- Important factor to identify delayed neutron and better reconstruct their energy.
- To separate close by showers and reduce the confusion for a better PFA application.

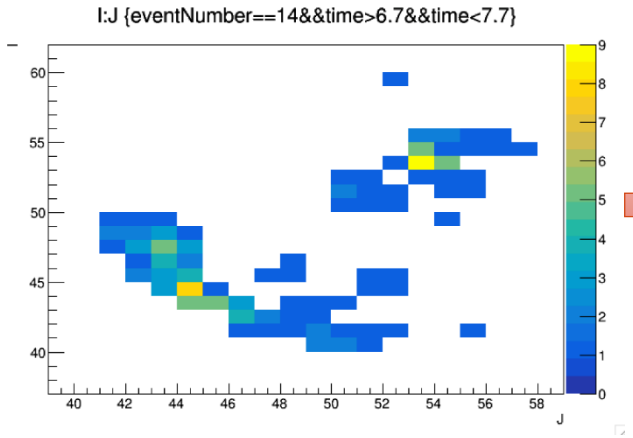
With Neutrons



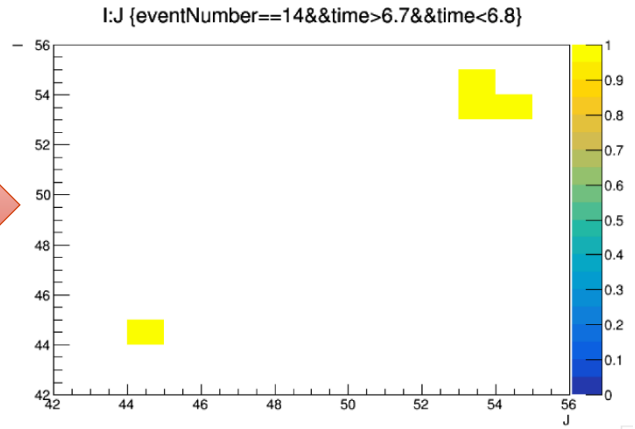
Without Neutrons



1 ns resolution



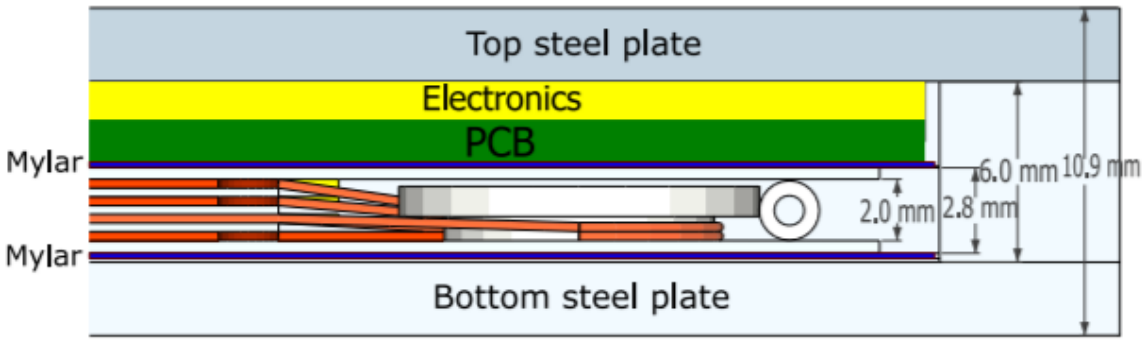
100ps resolution



How to achieve fast timing

- Purpose: => Identify neutral and charged hadrons
- Position, Energy and **Timing** => 5D HCAL

- Adding MRPC layers in the SDHCAL
- Front-end board for MRPC readout
  - Charge and timing measurement
  - High resolution timing measurement



✓ First step:

Design a front-end prototype board with four PETIROC2B chips

➢ Second step:

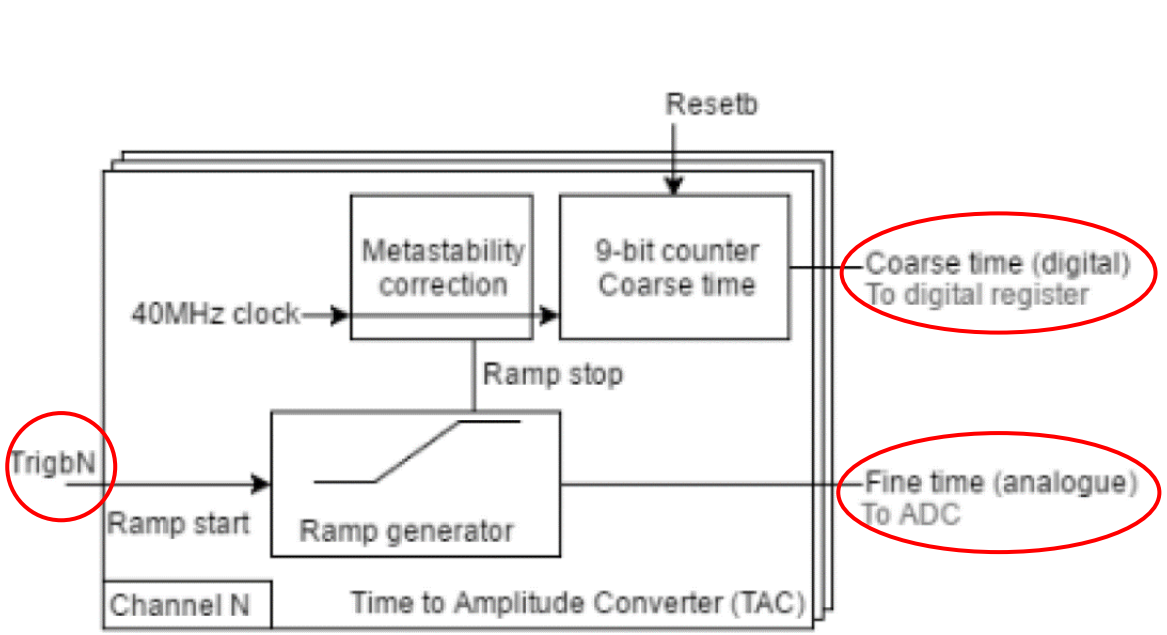
Build the 1m×1m **PETIROC2B FEE**

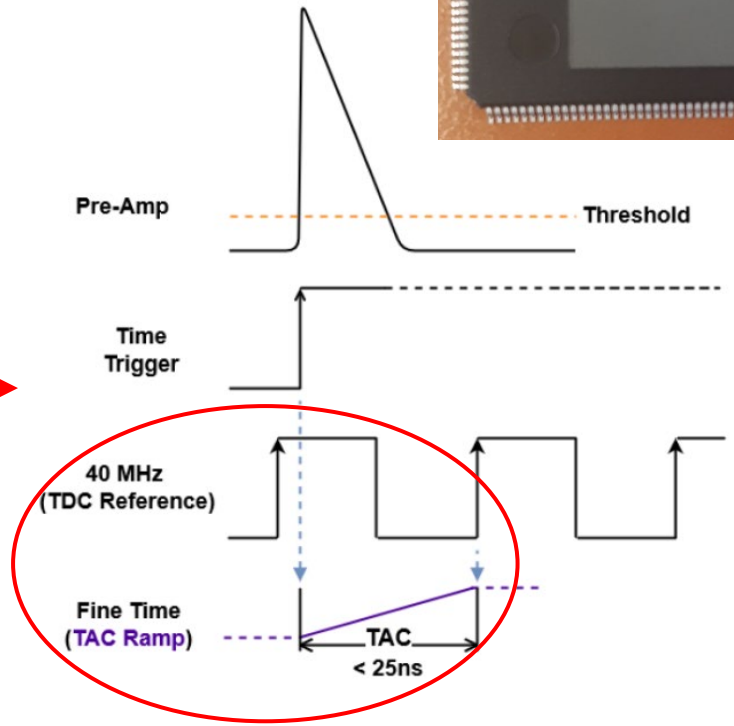
Introduction of Petiroc2B

- Time measurement
  - Coarse time is from a counter
  - Fine time by interpolating 40MHz
  - Jitter ~18 ps RMS on trigger output

  (4 photoelectrons injected)

- Charge measurement
  - 32chs input connected with PAD (readout unit)
  - Variable time shaper
  - Digitized with a 10bit ADC



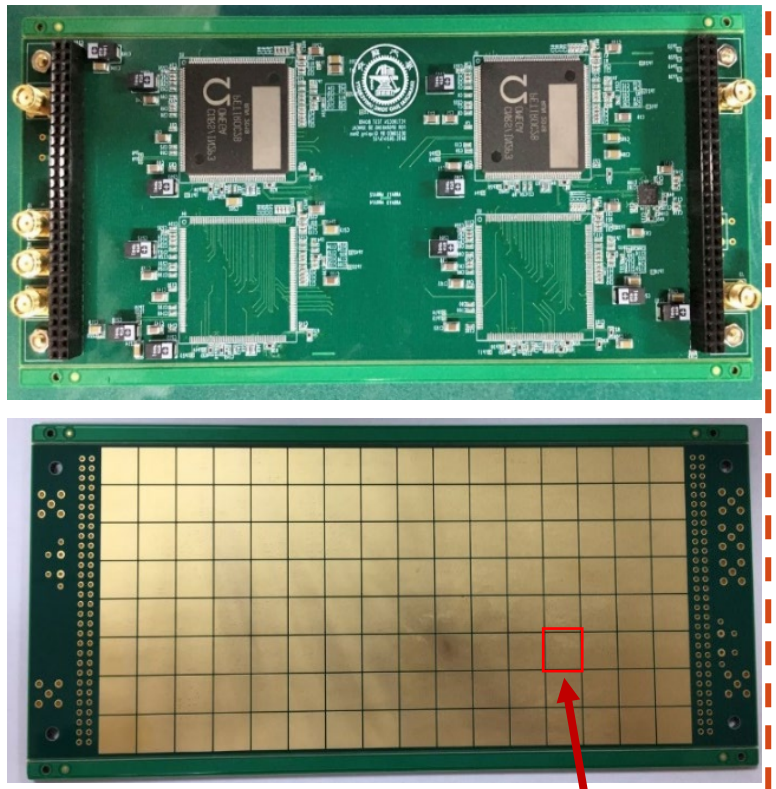


Front-End Electronics design

- 12 layers and 4 PETIROC chips.
- Many key induction units are at the bottom of the board.
- Via technology:
  - **Laser-drilled Via-in-pad** Technology (small size: ~0.1mm)
  - **Buried vias** with the size 0.3mm
  - **Through vias** located in two edges without induction pads

1		SURFACE	AIR
2	TOP	CONDUCTOR	COPPER
3		DIELECTRIC	FR-4
4	GND1	CONDUCTOR	COPPER
5		DIELECTRIC	FR-4
6	SIG1	CONDUCTOR	COPPER
7		DIELECTRIC	FR-4
8	SIG2	CONDUCTOR	COPPER
9		DIELECTRIC	FR-4
10	GND2	PLANE	COPPER
11		DIELECTRIC	FR-4
12	VDDA	PLANE	COPPER
13		DIELECTRIC	FR-4
14	VDDD	PLANE	COPPER
15		DIELECTRIC	FR-4
16	GND3	PLANE	COPPER
17		DIELECTRIC	FR-4
18	SIG3	CONDUCTOR	COPPER
19		DIELECTRIC	FR-4
20	SIG4	CONDUCTOR	COPPER
21		DIELECTRIC	FR-4
22	GND4	CONDUCTOR	COPPER
23		DIELECTRIC	FR-4
24	BOTTOM	CONDUCTOR	COPPER
25		SURFACE	AIR

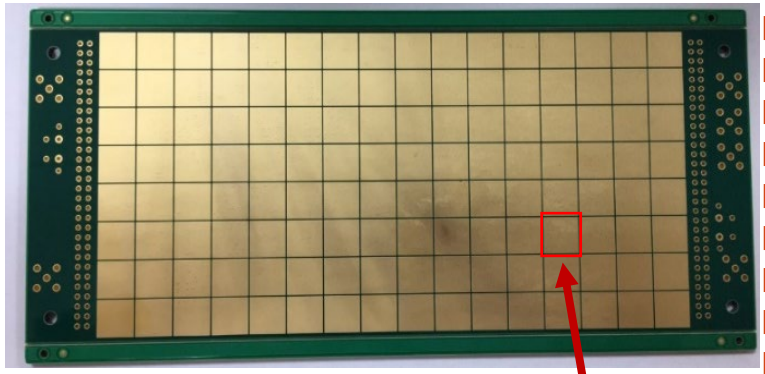
Stack-up and via layer design



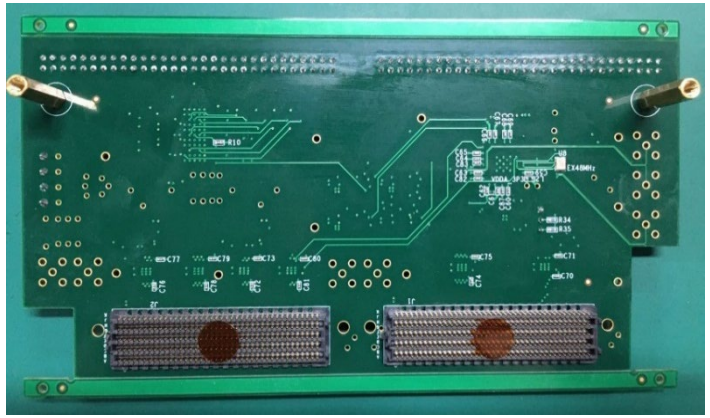
FE Board

Hardware prototype

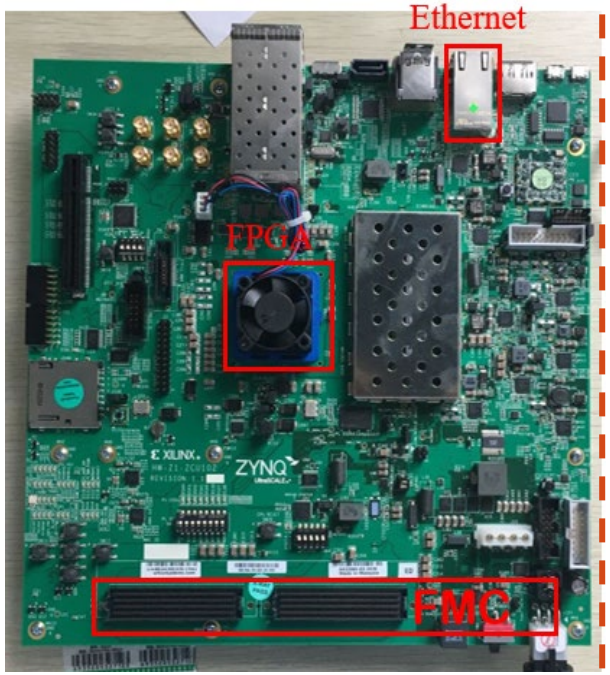
- Front End Board, Detector Interface Board, ZCU102 (Zynq UltraScale+ MPSoC).



FE Board



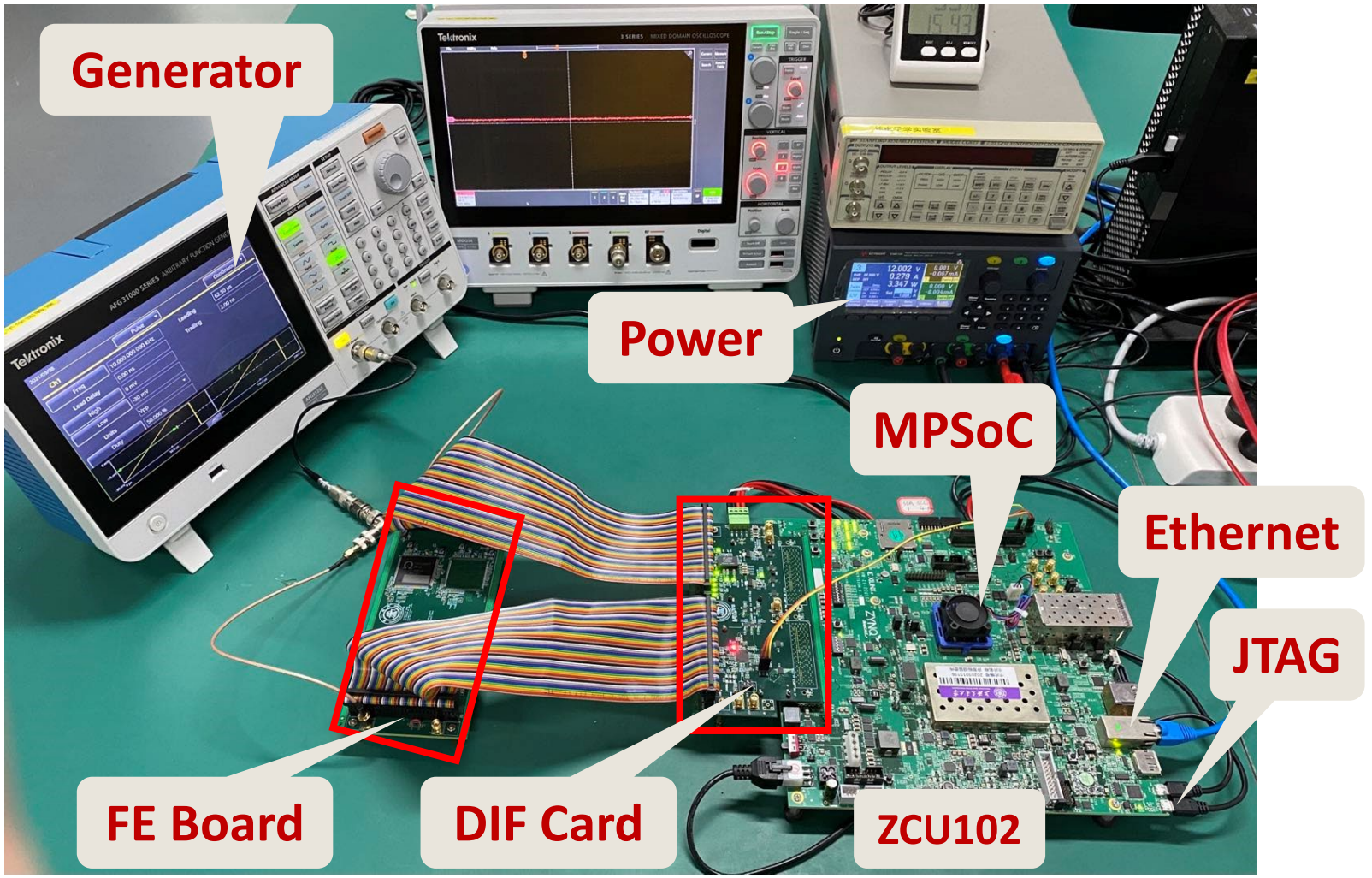
DIF Card



ZCU102

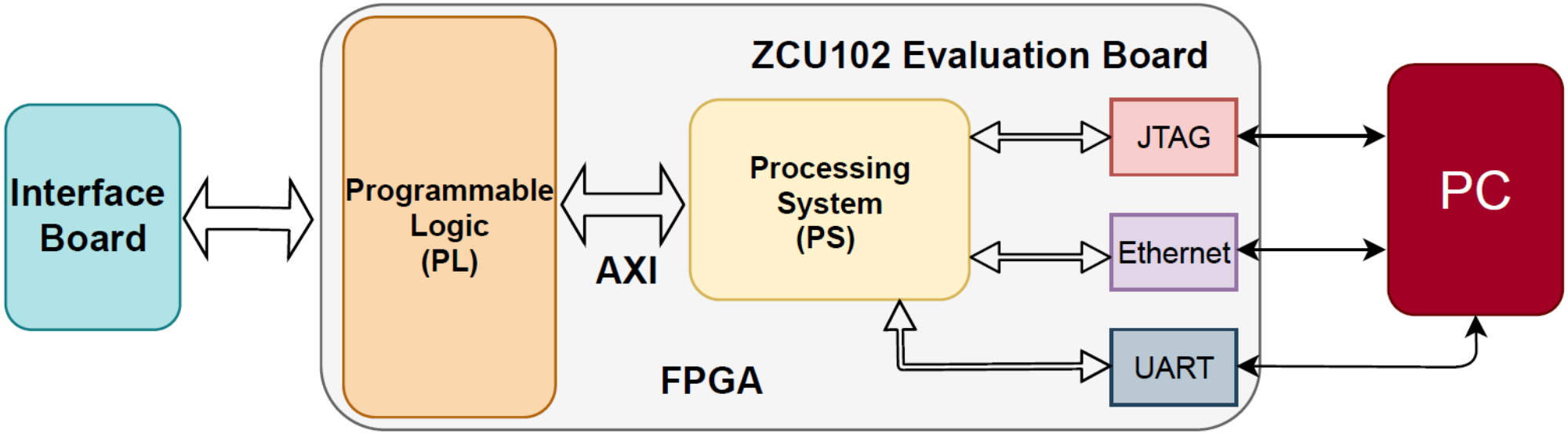
Prototype board test setup

- The setup picture for the injection test.
- **FEE, DIF, DAQ** are based on ZCU102.
- Status of the platform:
  - Configuration of PETIROC
  - Data transmission between FEB, FPGA and PC
  - Performance test of petiroc2b chips, timing measurement by injected signal



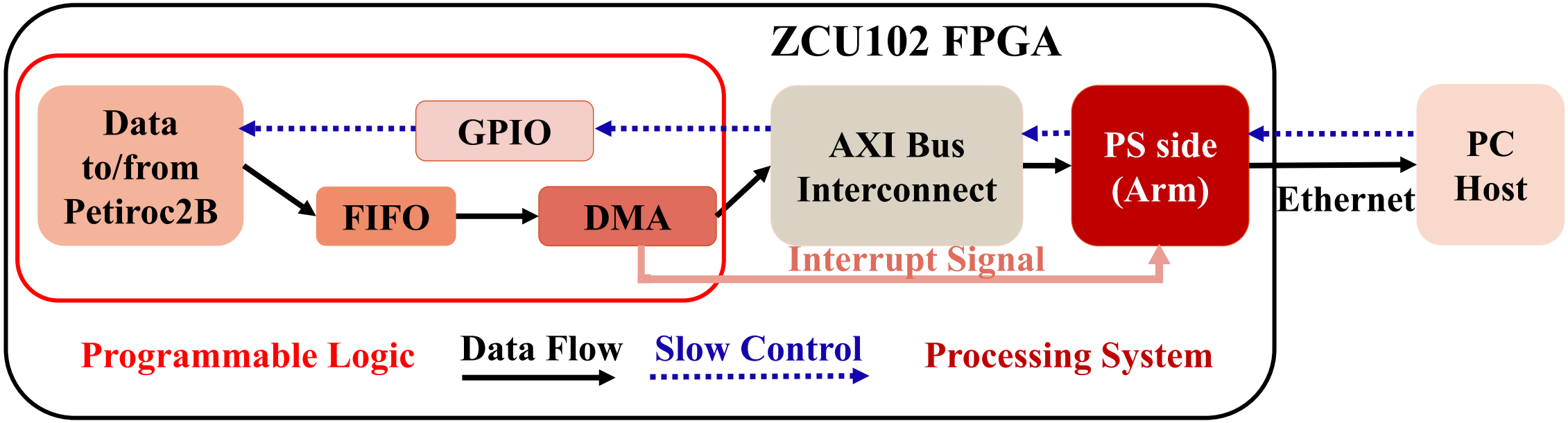
Data acquisition system

- The system is based on Xilinx ZCU102(FPGA) that contains Processing System(PS) and Programmable Logic(PL) <= (Xilinx Vivado 2019.2 and Vitis IDE).
  - The UART communication of FPGA and PC
  - Ethernet communication between FPGA and PC used to transfer data
  - Data transmission with AXI bus and DMA between PS and PL, inside of ZCU102



Firmware

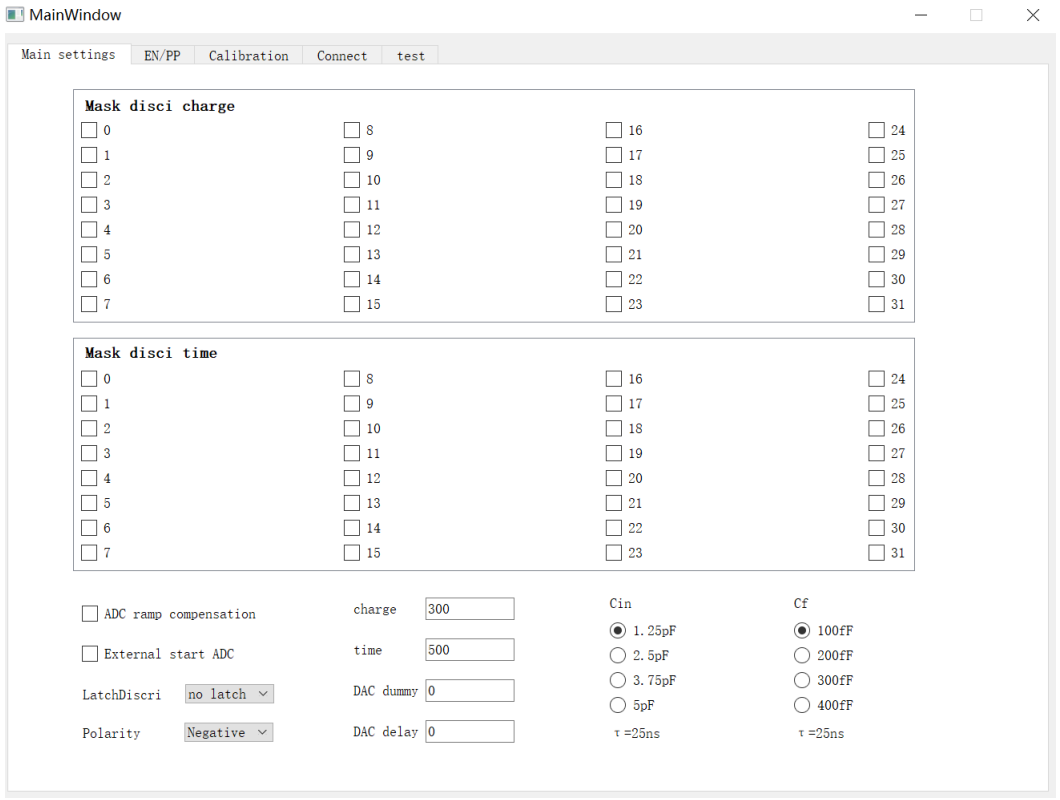
- Flow chart for slow control and data transmission.
- The implementation of the firmware is in the programmable logic while the control part is implemented on the processing system inside ZCU102.



Software

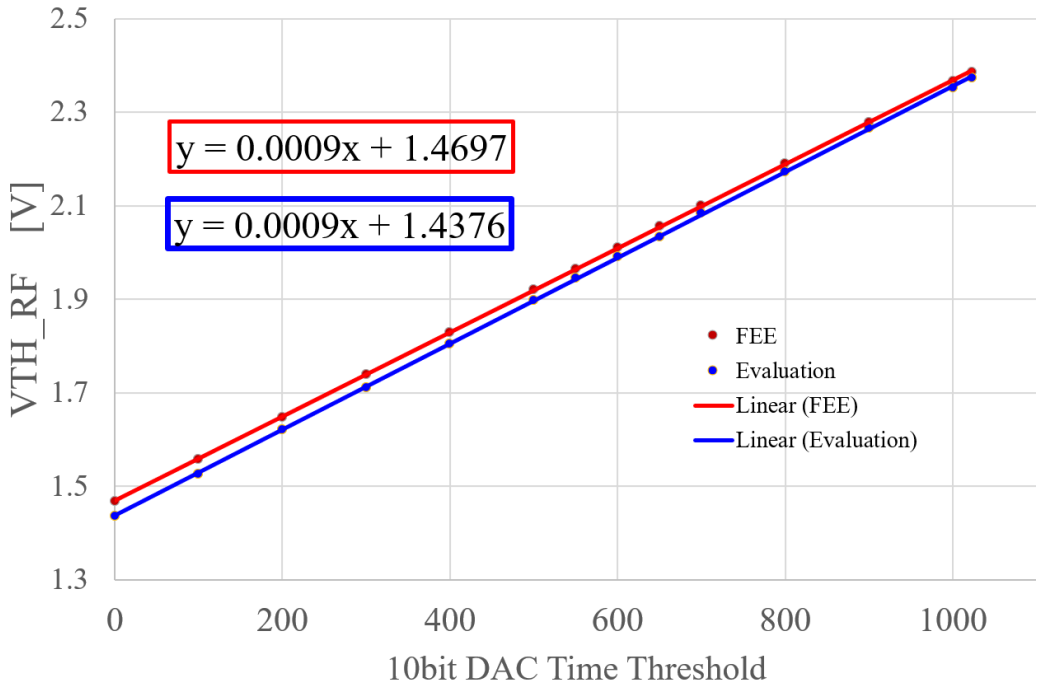
- Software developed with python language by QtCreator
- The configuration set in the software and sent to the FPGA over ethernet with TCP
- Data received from FEB, saved to the PC side.

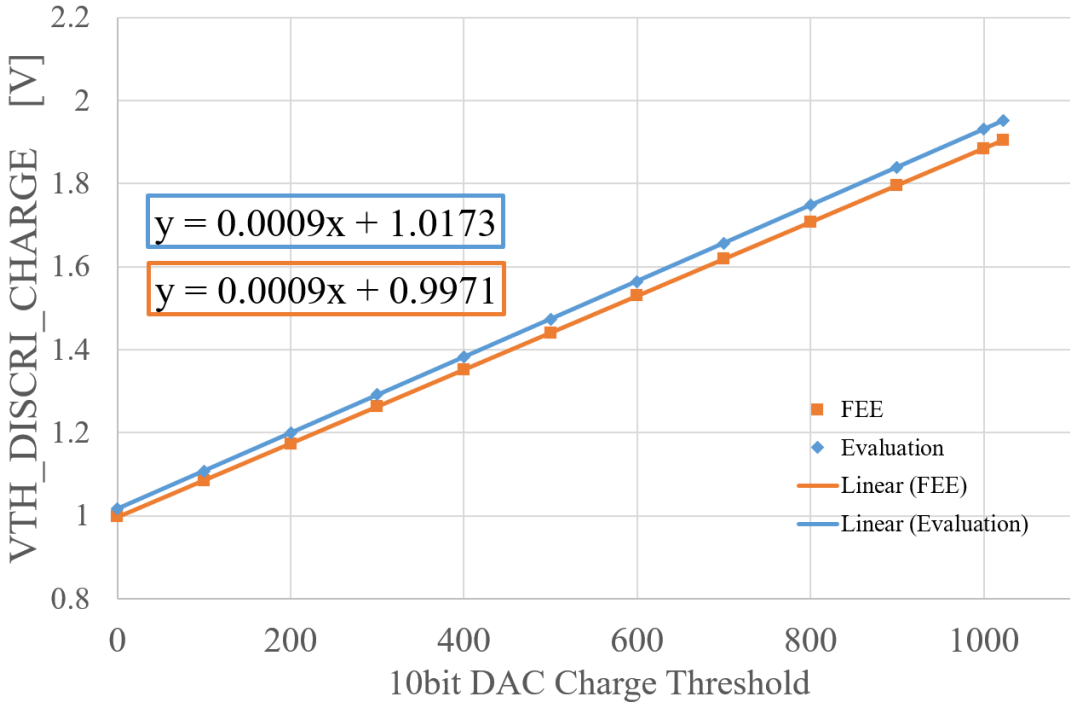
Yihan Guo



Time and charge threshold voltage test

- Time threshold is correct according to the voltage value with 10bit DAC.
- Configuration of Petiroc2B is also right.
- Differential pairs (Dout n/p) are used to take data.





- Time and Charge threshold can be well controlled.

Summary and ongoing works

- ✓ The signal injection test setup has been finished.
- ✓ The preliminary DAQ system based on ZCU102 has been designed.
  - ✓ The configuration of the petiroc2b checked and correct.
  - ✓ The decode of output data from the FEB implemented.
  - ✓ The DAQ system works well but still under improvement.

Future plans:

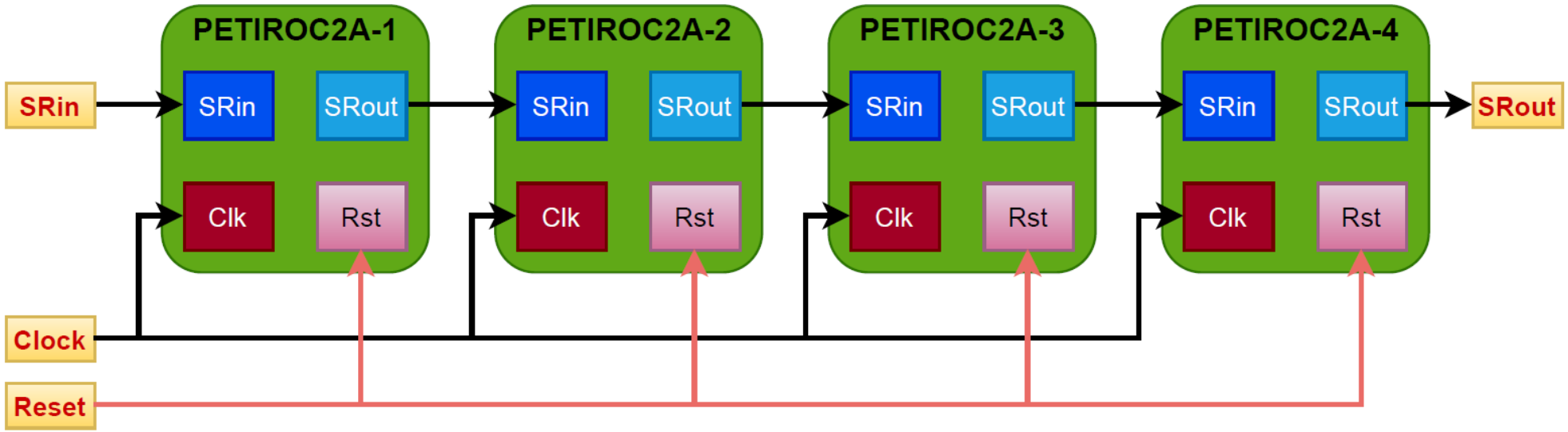
- ☐ Take some measurements to decrease noise.
- ☐ Perform the calibration for Petiroc2b channels.
- ☐ Signal injection test to analyze the timing performance of Petiroc2B.
- ☐ Further improve the DAQ system and the software GUI.

Thanks for your attention!

Backup Slides

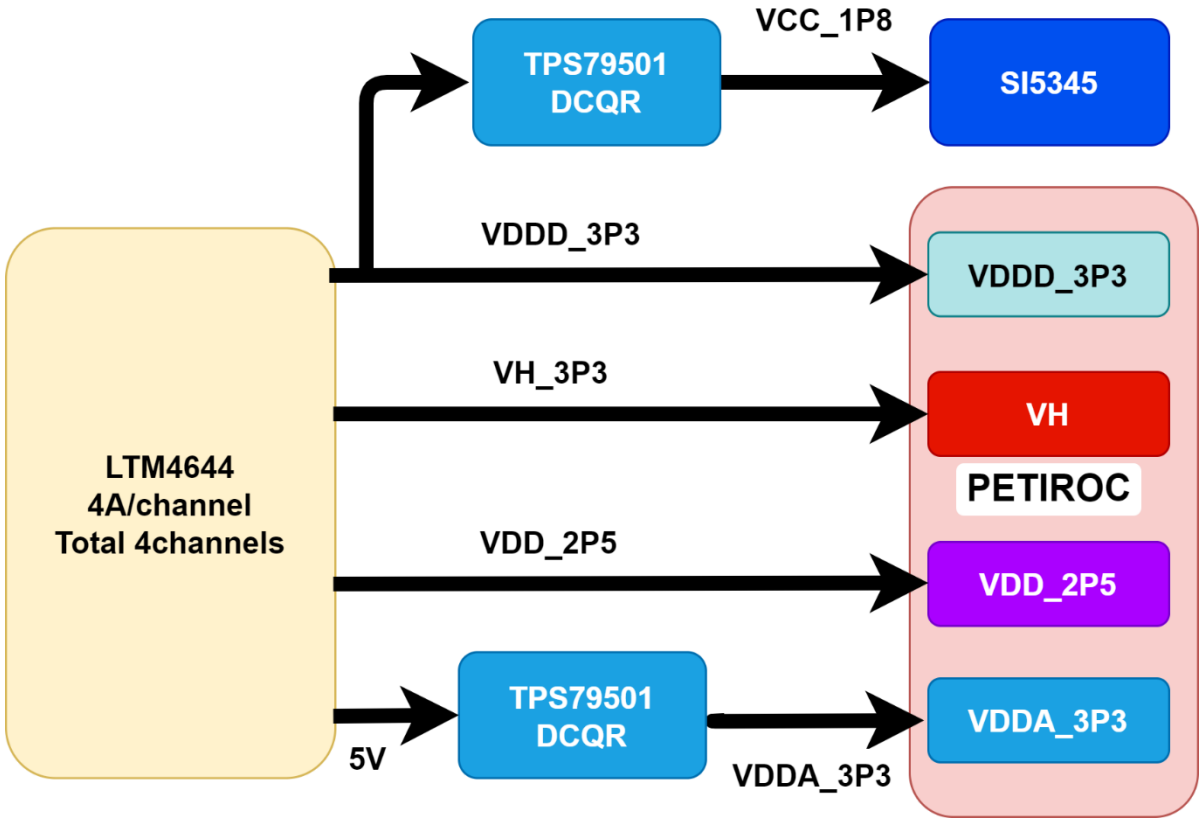
Sub-component Design

- Front-End readout Board Design
- Components: 4 Petiroc2B, clock buffer, 2 headers, SMA for signal injection .
- 128 pads at the bottom, induction unit size: 1cm×1cm.
- The dimension:197mm*82mm, the blind/buried via technology.
- Configuration for petiroc2a with daisy-chain (SPI sending shift register data)

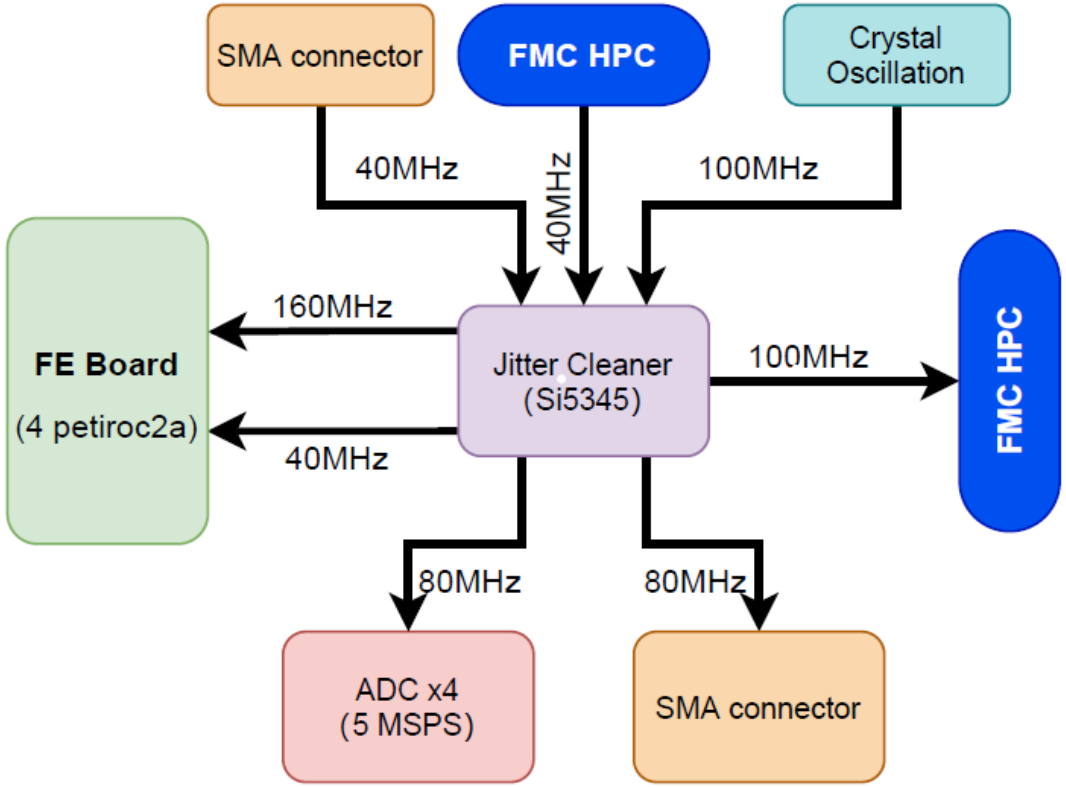


Details on DIF Design

- Detector Interface Card Design: mainly jitter cleaner and power system



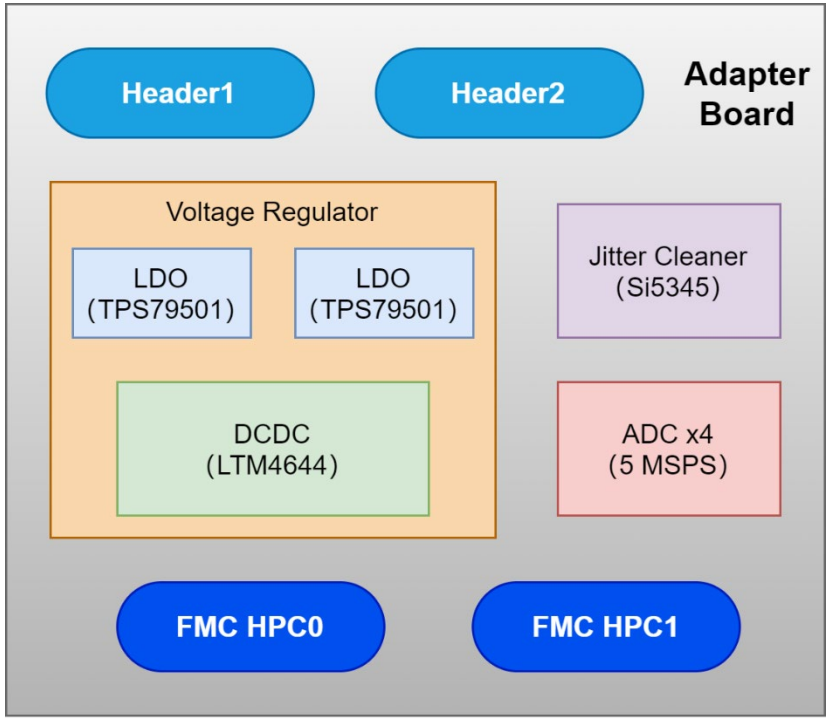
Block diagram of Power Rail



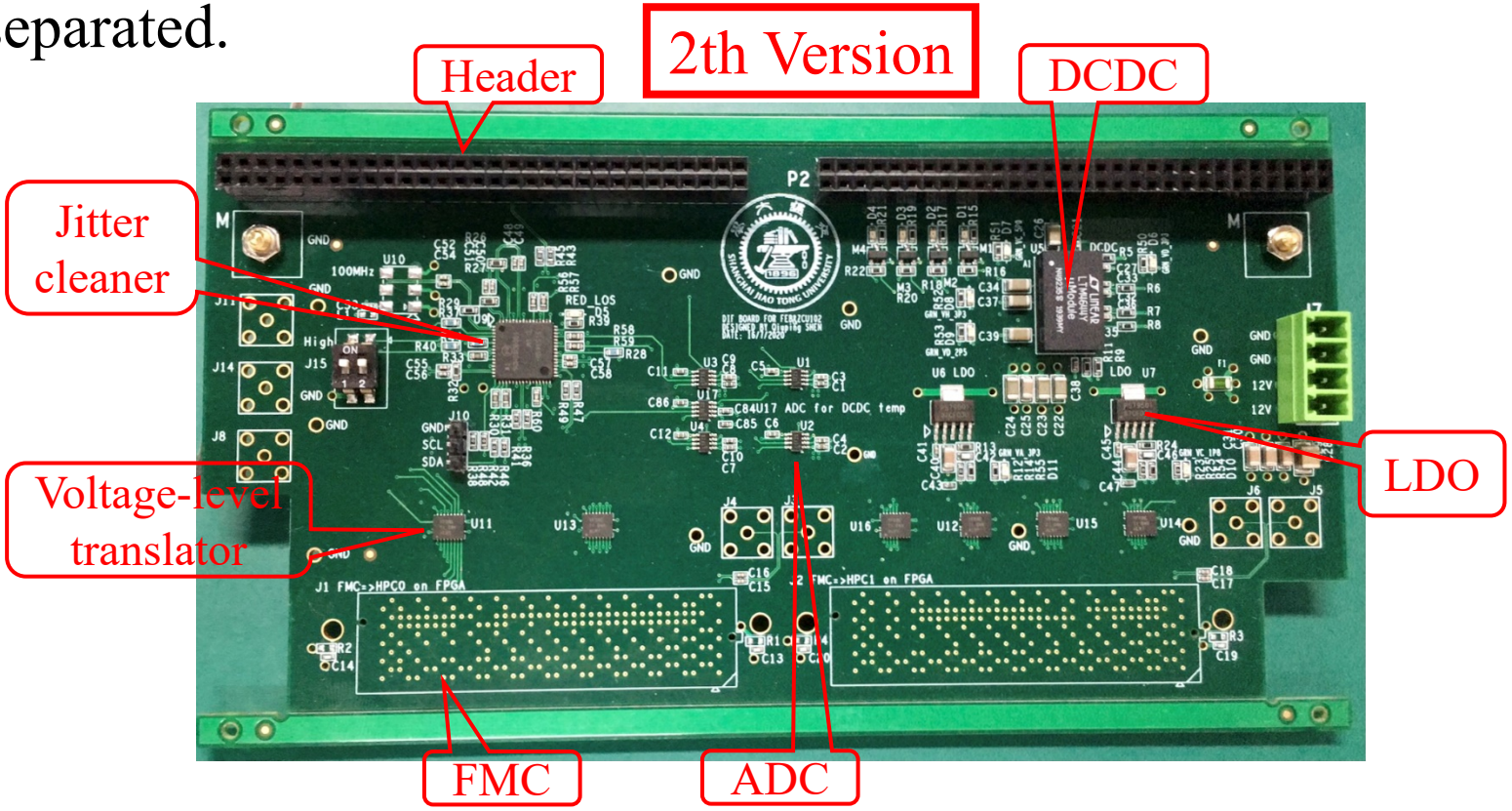
Block diagram of Clock

Sub-component Design

- Detector Interface Card Design: mainly jitter cleaner and power system
- DIF card will be in charge of the communication and data transfer with the FE electronics(two headers) and ZCU102(two FMCs).
- Analog and digital power are separated.

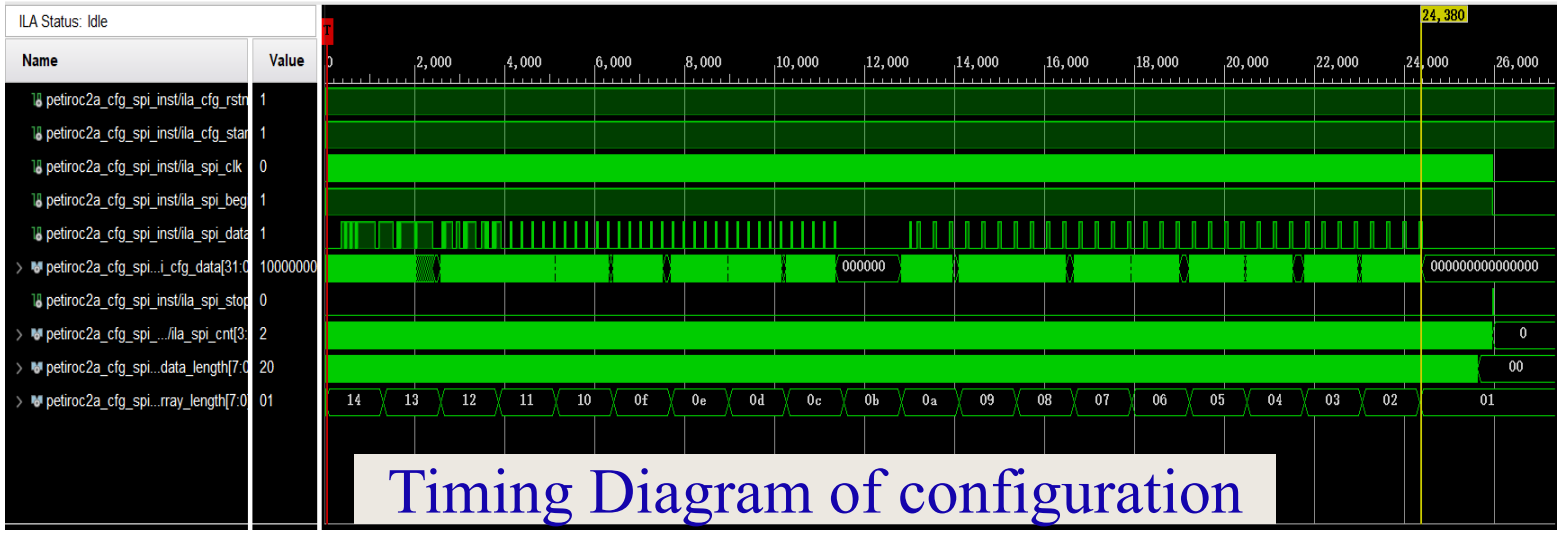


More Details

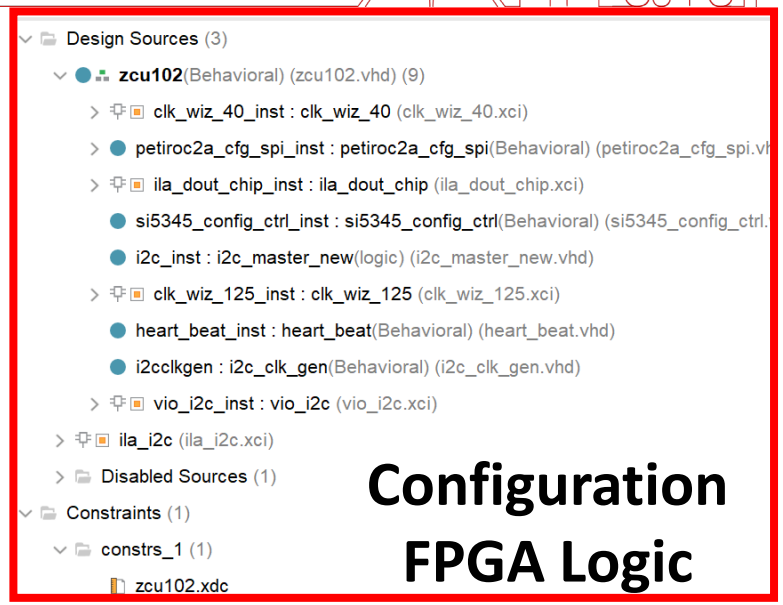


PETIROC chips configuration

- 648 bits data with SPI method is sent to Shift Register inside PETIROC.
- PETIROC configuration works well.
  - All bias voltage values are correct.
  - Output data has been checked, after sending trigger signals



Timing Diagram of configuration



Configuration FPGA Logic

Bias Voltage	Value(V)
vref_inpdac	0.989
vref_time	1.664
vref_charge	0.976
vref_tdc	0.133
vref_adc	0.961
vref_time_pad	1.658